

ADVANCED GAN DEVICES AND TECHNOLOGY FOR RF AND POWER
SWITCHING APPLICATIONS

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ADVANCED GAN DEVICES AND TECHNOLOGY FOR RF AND POWER SWITCHING APPLICATIONS

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GaN-based devices show great potential for high-speed RF power applications as well as power switching applications due to the high electron velocity and high breakdown field in GaN over Si, GaAs and SiC. Another unique property of III-V nitride materials (GaN, AlN, InN) is polarization, which can be engineered to induce 2-dimensional electron gas (2DEG) at heterojunction interfaces as well as induce 3-D electron gas in thick (bulk) layers by grading the alloy composition of the layers, e.g. AlGaN, without impurity doping. This unconventional doping scheme is termed as polarization-doping or Pi-doping. This work focuses on device development and proposals to advance GaN technologies for RF and power switching applications.

During the quest to realize THz GaN transistors, it has been identified that the ultimate factors limiting the GaN high electron mobility transistors (HEMTs) are the intrinsic transconductance (g_m) and the fringing capacitance ($C_{fringing}$) associated with the T-gate: speed $\propto g_m/C_{fringing}$. In InAlN/GaN HEMTs, the device current gain cut-off speed is increased from 230 GHz to >300 GHz by reducing $C_{fringing}$ and further increased to ~ 400 GHz by improving g_m . Effects of scaling the source-drain distance on ultra-scaled devices are also studied.

Low leakage and low current collapse (or frequency dispersion) are crucial for transistors. A record-low leakage of 1×10^{-12} A/mm simultaneously with a low current collapse is achieved in AlGaN/GaN-on-Si HEMTs employing the regrown ohmic contact technology. The device improvement is attributed to the contact regrowth

since generation of surface traps is minimized by avoiding the conventional high temperature annealing process to form alloyed ohmic contacts.

For high-voltage high-current power switching applications (>100 kW), vertical devices are highly desirable over lateral ones. To this end, we have proposed a series of GaN devices grown on bulk GaN substrates and employing the unique feature in the GaN material family - polarization doping. Analytical modeling suggests that at the same breakdown voltage, a up to 2x lower specific on-resistance ($R_{on,sp}$) can be achieved in Pi-doped devices compared to impurity doped GaN power devices. High voltage impurity and Pi-doped GaN p-n diodes with a breakdown voltage (BV) >1.2 kV and avalanche breakdown capability have been developed experimentally. Another concept called GaN Lateral Polar Super Junctions (LPSJ) is also proposed and theoretically analyzed, featuring uniformly Pi-doped n/p-pillars to overcome the conventional tradeoff between BV and $R_{on,sp}$ in a unipolar drift region of a power device. The design space for GaN LPSJs is explored using a 2D analytical model of BV and $R_{on,sp}$ under both charge balanced and imbalanced conditions.

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Journal Publications

1. B. Song, M. Zhu, G. Xing et al, “Unipolar Figure-of-Merit of Polarization-Doped GaN Power Devices,” *J. Appl. Phys.*, submitted
2. B. Song, M. Zhu, Z. Hu, M. Qi, K. Nomoto, X. Yan, Y. Cao, D. Jena, and H. Xing, “Ultralow Leakage AlGaIn/GaN High Electron Mobility Transistors on Si with Non-alloyed Regrown Ohmic Contacts,” *IEEE Electron Device Lett.*, vol. 37, no. 1, pp. 16–19, 2016 (News in Semiconductor Today).
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Research Interests

GaN high-speed and high-power device design, simulation, fabrication, characterization, and analysis.

Dedication to my parents and Lin

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CHAPTER 1

INTRODUCTION

1.1 III-nitride Materials for RF and Power Switching Applications

Owing to the high electron velocity and high critical breakdown field, GaN based devices attracted great attention for both RF and high-voltage power applications. GaN High Electron Mobility Transistors (HEMTs) provide a high two-dimensional electron gas (2DEG) density on the order of 10^{13} cm^{-2} due to strong polarization effects and a modest electron mobility up to $2200 \text{ cm}^2/\text{V.s}$, which results in an output current density over 4.0 A/mm [1] and in turn a high output power density at a large power supply voltage. Moreover, the high thermal conductivity $2.6 \text{ W}/(\text{cm} \cdot \text{K})$ of GaN has also been reported recently compared to 1.5 and $\sim 3.5 \text{ W}/(\text{cm} \cdot \text{K})$ of Si and SiC, respectively[2]. Together with the usage of a high thermal conductivity SiC substrate, it can greatly reduce packaging and cooling costs for the same chip output power in comparison with technologies based on Si and GaAs. These features of GaN enable small-footprint power amplifications with high power-added-efficiency in cellular devices, base stations, wireless networks and defense systems. For example, over 30 W/mm output density at 8 GHz in the X-band [3] and 3 W/mm output density at 96 GHz in the W-band [4] have been reported. A more comprehensive review on GaN HEMTs for RF power applications can be found in Ref. [5]. GaN HEMT cutoff frequencies are significantly increased recently by great efforts from several groups. I-gate InAlN HEMTs with a gate length of 30 nm showing a maximum current gain cutoff frequency (f_T) of $370\text{-}400 \text{ GHz}$ have been demonstrated by our group [6], [7].

More recently, 20 nm T-gate AlN/GaN HEMTs with balanced f_T and maximum oscillation frequency (f_{max}) in the range of 450 GHz have been reported by HRL [8], [9]. The improvement in the device speed is accomplished through innovative device scaling technologies such as self-aligned-gate (SAG) processes [1], [8]–[11], n+-GaIn ohmic contact regrowth [12], [13], thin AlN top barriers [14],[15], thin InAlN top barriers [6], [7], [16], AlGaIn or InGaIn back barriers [17], [18], or HEMTs on N-polar GaN HEMT [19]–[21]. The state-of-art high-speed GaN HEMTs reported by different groups have been summarized in Fig. 1.1[22].

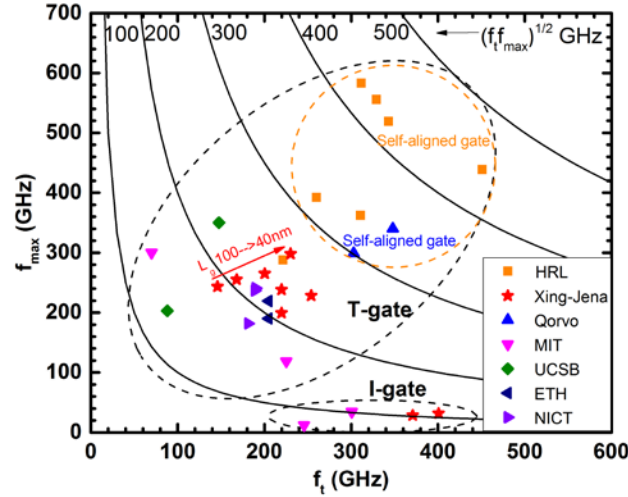


Figure 1.1 Comparison of high speed performance of the state-of-the-art GaN HEMTs reported by different groups [22].

For power switching applications, Si power device performance after several decades' development is reaching the intrinsic material limits of Si. Wide band gap (WBG) semiconductors such as SiC and GaN are emerging for the next generation power switching due to the higher voltage/higher current, lower power loss, higher frequency and higher temperature capabilities compared to Si. Thus more compact and efficient power converters are possible using WBG semiconductors. Table 1.2 is

a summary of the material properties of various semiconductors for power switching applications. When comparing the Baliga's Figure of Merit (BFOM) of different materials, we can find that the BFOM of SiC and GaN are two orders of magnitude higher than that of Si. Thus, SiC and GaN promise substantially lower specific on-resistance as shown in Fig. 1.2, where the unipolar limits of the breakdown voltage (BV) and on-resistance of power devices for various materials are illustrated. WBGs such as β -Ga₂O₃ ($E_g \sim 4.9$ eV), diamond ($E_g \sim 5.5$ eV) and AlN ($E_g \sim 6$ eV) have even higher BFOMs, thus ideally they would also be attractive for power switching applications. However, due to the challenges in the high-quality material development, they are now in the very early development stage for power switching applications [23]–[25].

Table 1.1 Material properties of various semiconductors

<i>Semiconductor Properties</i>	Si	GaAs	4H-SiC	GaN	β -Ga ₂ O ₃	Diamond	AlN
E_g (eV)	1.12	1.42	3.26	3.4	4.8-4.9	5.5	6
E_{br} (MV/cm)	0.3	0.4	3	3.3	8	10	15
v_{sat} (10⁷ cm/s)	1	1	2	2.5	-	2.7	-
μ_n (cm²/Vs)	1400	8500	1000	1200	300	2000	500
T (W/cm K)	1.5	0.43	3.3-4.5	2.6*	0.13-0.23	20	2.85
ϵ	11.8	12.9	9.7	9.0	10	5.5	8.5
BFOM $\epsilon\mu E_{br}^3$	1	14	340	870	3444	24664	32158

*N. Killat, "Thermal Properties of AlGaIn/GaN HFETs on Bulk GaN Substrates", *EDL*, 33, 366 (2012). In the past few years, GaN-based lateral power switching transistors with breakdown voltage (BV) ratings > 600 V have started being adopted in power systems [26]–[28]. However, development of the GaN vertical power devices lagged behind due to the unavailability of high-quality and high-quantity GaN bulk substrates. This

situation is being transformed dramatically in the recent years since both the GaN-based laser/lighting industry as well as the power electronics industry demand GaN bulk substrates [29], [30]. GaN grown on sapphire, SiC or Si substrates, typically possesses a high density of defects thus leading to device performance far below expectation.

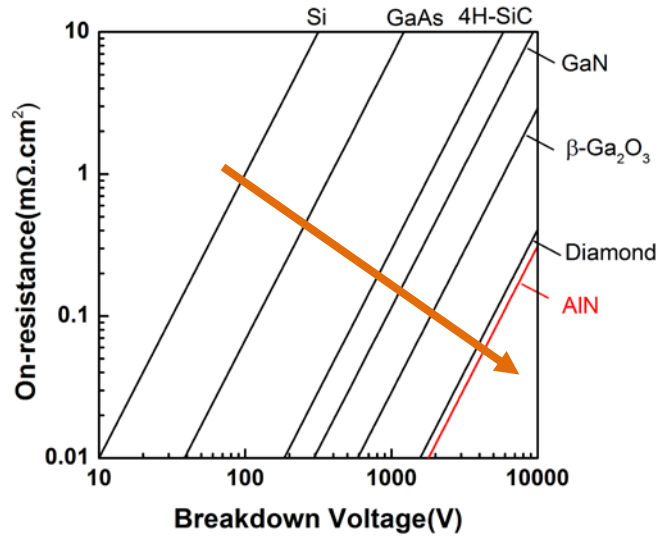


Figure 1.2 Comparison of the unipolar specific on-resistance versus BV in power devices for different materials. The material parameters used are from Table 1.1.

1.2 Polarization Induced Charges in III-nitride Heterostructures (2DEG) and AlGaN Graded Layers (bulk Pi-doping)

Besides the aforementioned advantages of GaN, another unique property of *III-N* materials is the strong spontaneous and piezoelectric polarization. The GaN crystal exhibits a large spontaneous polarization along the c -axis ([0001] direction) and piezoelectric polarization under strain due to the non-centrosymmetry of the wurtzite lattice structure, shown in Fig. 1.3. Fig. 1.4 shows the dipole formation in a unit cell

due to the spontaneous polarization P_{sp} and the net charge for a freestanding GaN slab at the bottom and top surfaces [31]. For the piezoelectric polarization P_{pz} , it can be expressed by:

$$P_{pz} = 2(e_{31} - e_{33} \frac{C_{13}}{C_{33}})\varepsilon \quad (1.1)$$

where e_{31} , e_{33} are the piezoelectric coefficients, C_{13} , C_{33} are the elastic constants, and ε is the in-plane strain by:

$$\varepsilon = \frac{a - a_0}{a_0} \quad (1.2)$$

where a and a_0 are the lattice constants of the strained layer and the substrate, respectively. The total polarization (P_T) is then given by

$$P_T = P_{sp} + P_{pz} \quad (1.3)$$

The polarization related material parameters of AlN, GaN and InN are summarized in Table 1.2 [32]. Material properties of ternary and quaternary alloys can be determined by linearly interpolating these constants.

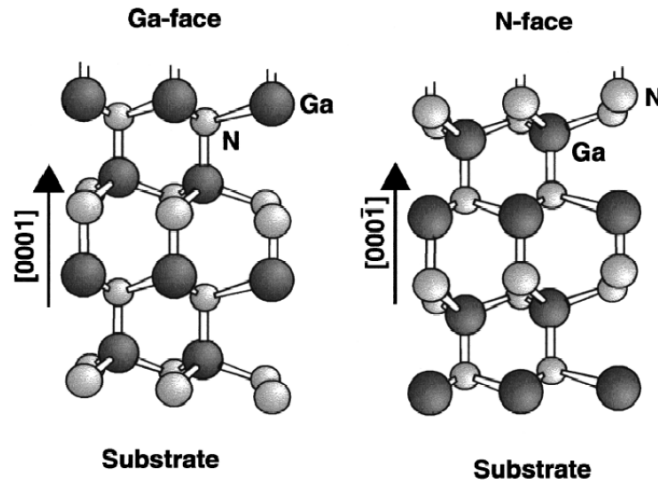


Figure 1.3 Schematic crystal structures of wurtzite Ga-face and N-face GaN[31]

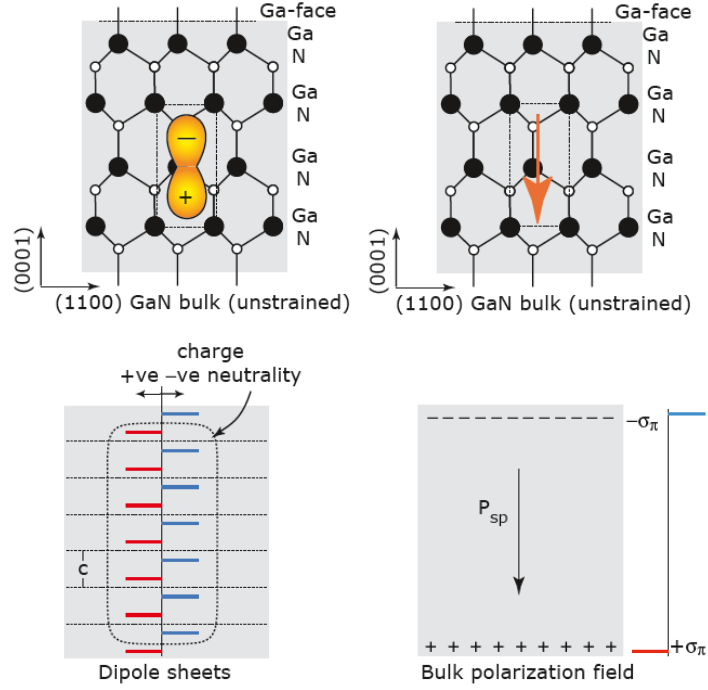


Figure 1.4 Microscopic picture of spontaneous polarization in a freestanding GaN slab [31]

Table 1.2 MATERIAL PARAMETERS OF WURTZITE AlN, GaN AND InN [32]

<i>Semiconductor Properties</i>	InN	GaN	AlN
E_g (eV)	0.7	3.4	6
a_0/c_0 (Å)	3.544/5.718	3.189/5.185	3.111/4.978
P_{SP} (C/m ²)	-0.032	-0.029	-0.081
e_{33} (C/m ²)	0.97	0.73	1.46
e_{31} (C/m ²)	-0.57	-0.49	-0.6
C_{13} (GPa)	92	103	108
C_{33} (GPa)	224	405	473

Fig. 1.5 shows the spontaneous and piezoelectric polarization directions in Ga-face AlN/GaN and InN/GaN heterostructures. Since pseudomorphic InN and AlN layers on GaN are under opposite strain, the piezoelectric polarization in these two cases are opposite. Fig. 1.6 shows an AlGaIn/GaN HEMT structure, where the difference in the polarization in GaN and AlGaIn leads to a positive bound sheet charge, which in turn attracts negative mobile charges to create a two-dimensional electron gas (2DEG) at this interface to satisfy the charge neutral rule over the entire semiconductor structure. Since the 2DEGs are realized without impurity doping, high mobility are preserved. The amount of charges in the 2DEG channel can be determined using the energy band diagram. The conduction band diagram was calculated by a self-consistent solution of Schrodinger and Poisson's equations by a 1D Poisson solver. By assuming that only the first sub-band with a ground state energy level (E_0) is occupied,

$$E_F - E_0 = \frac{\pi \hbar^2 n_s(x_{Al})}{m^*} \quad (1.4)$$

where E_F is the Fermi level, we can estimate the 2DEG density n_s from the band diagram. With a barrier thickness of t_b , the electric field F in the AlGaIn barrier can be determined by

$$F = \frac{q(\sigma_\pi(x_{Al}) - n_s(x_{Al}))}{\epsilon_r \epsilon_0} \quad (1.5)$$

where $\sigma_\pi(x_{Al})$ is the net polarization charge at the interface and $n_s(x_{Al})$ is the 2DEG charge at the quantum well. With the conduction band discontinuity ΔE_c at AlGaIn and GaN, we can get the following relationship from Fig. 1.6

$$q\phi_s - qFt_b - \Delta E_c + E_0 + (E_F - E_0) = 0 \quad (1.6)$$

where ϕ_s is the barrier height with respect to the metal. From eq. (1.4)-(1.6), we can get $n_s(x_{Al})$ as a function of the AlGa_N barrier thickness t_b and Al composition x_{Al}

$$n_s(x_{Al}) = \frac{(\Delta E_c - E_0 - q\phi_s + \frac{q^2 \sigma_\pi(x_{Al}) t_b}{\epsilon_r \epsilon_0})}{(\frac{q^2 t_b}{\epsilon_r \epsilon_0} + \frac{\pi \hbar^2}{m^*})} \quad (1.7)$$

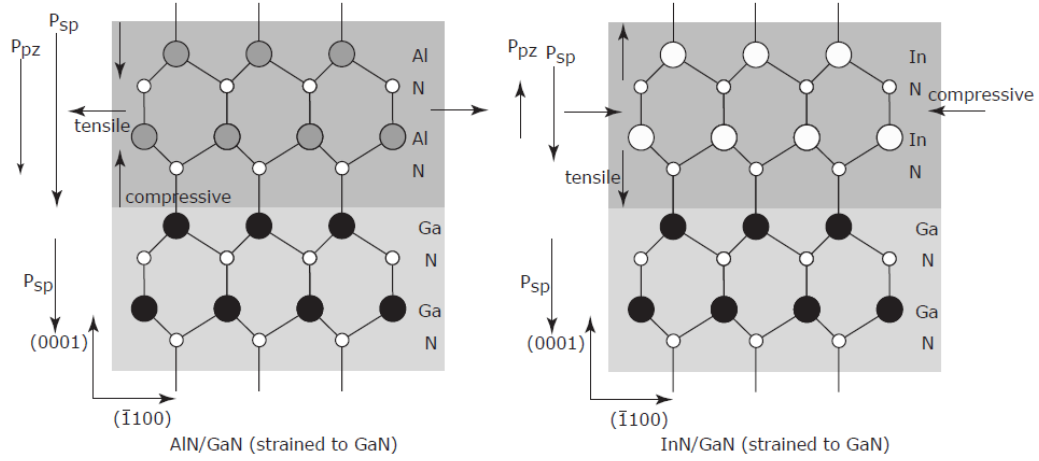


Figure 1.5 Spontaneous and piezoelectric polarization and their directions in GaN, InN and AlN [32]

A review of the fundamentals on polarization doping is shown in Fig. 1.7 and Fig. 1.8. On the Ga-face GaN, when grading from GaN to AlGa_N, the difference in spontaneous and piezoelectric polarization charges in Al_xGaN to Al_{x+δ}GaN leads to a 3 dimensionally distributed positive charge in the crystal layer (Fig. 1.7) [31], [33]. These positive charges associated with the crystal lattice are immobile, in turn attracting mobile negative charges from surface donors or other states occupied by electrons including the valence band to minimize the electric field within the crystal layer (Fig. 1.8). In order to obtain mobile holes, one just needs to grade back from Al_xGaN to GaN on Ga face or grading from GaN to Al_xGaN on N face [34]. The

volume polarization charges $\rho_\pi(x_{Al})$ for a layer with a linear grading of the Al composition (GaN to Al_xGaN) over a thickness of d can be determined by

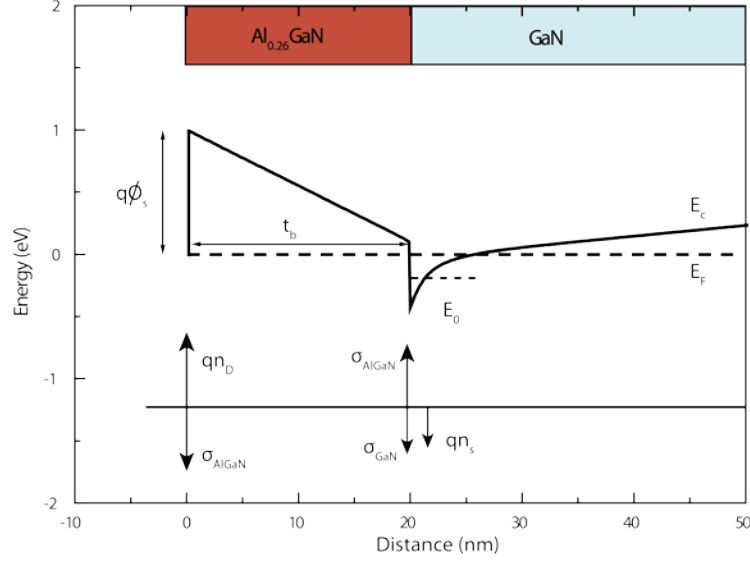


Figure 1.6 Conduction band diagram of $Al_{0.26}GaN$ /GaN HEMTs grown on [0001] GaN.

$$\rho_\pi(x_{Al}) = \frac{\sigma_\pi(x_{Al})}{d} \quad (1.8)$$

Its major difference from the conventional impurity induced doping is that the polarization-induced electrons (or holes) are *electric field ionized* but the impurity-doped electrons (holes) result from thermal excitation of electrons (holes) at the donor (acceptor) energy states to the conduction (valence) energy band of the semiconductor. As a result, the polarization-induced electrons do not suffer from carrier freeze-out as the impurity-doped electrons do when temperature decreases. Meanwhile, the polarization-doped electrons typically exhibit higher mobility due to the absence of

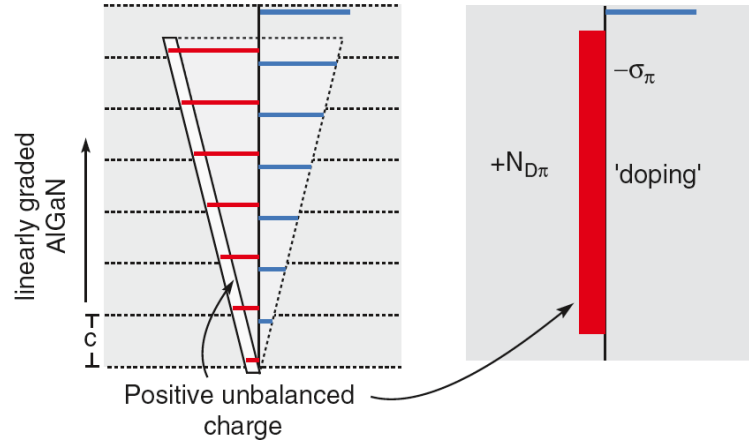


Figure 1.7 Illustration of formation of net bulk charges in a layer with polarization gradient [31]

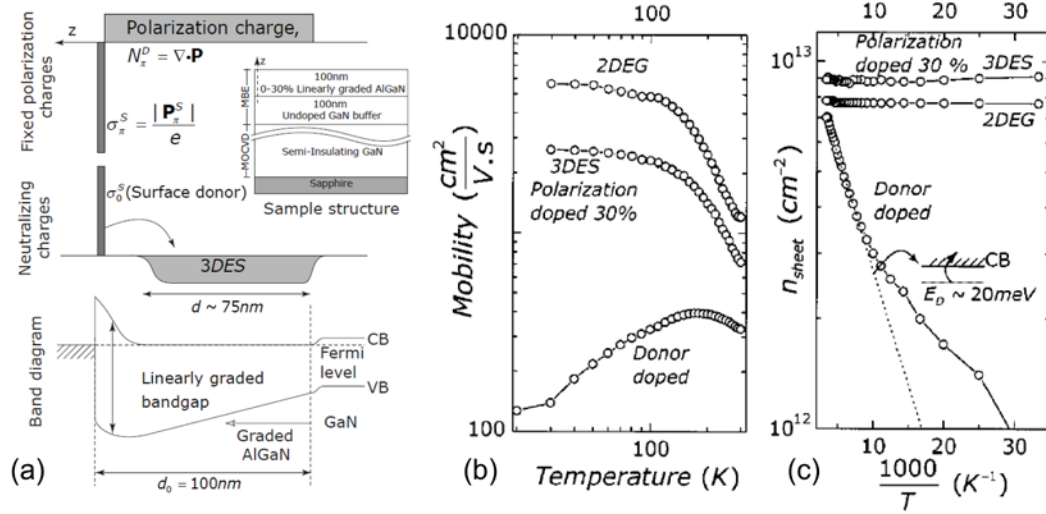


Figure 1.8 (a) Schematic of charge control showing polarization charges and formation of 3DES. A band diagram shows depletion of the 3DES due to surface potential. Also shown is the epitaxial layer structure that generates the 3DES. (b) Temperature-dependent carrier sheet densities and (c) carrier mobility obtained experimentally in 3 structures: a polarization-doped bulk, an impurity-donor-doped bulk and a 2DEG structure [33].

ionized impurity scattering [35]. Figure 1.9 shows the charge density as a function of the Al composition x and the graded-layer thickness d when x being linearly graded from GaN to Al_xGaN [36]. Also included are the reported experimental data. We can

see the past research was mainly focused on high carrier concentrations of $>10^{18} \text{ cm}^{-3}$, while for power switching applications, a doping concentration below 10^{17} cm^{-3} is highly desirable for achieving high breakdown voltages. To this end, a wide-open and unique research opportunity emerges to explore the low-concentration region by polarization doping, which can be conveniently coupled with high breakdown voltages afforded in Al_xGaN with a bandgap higher than that of GaN.

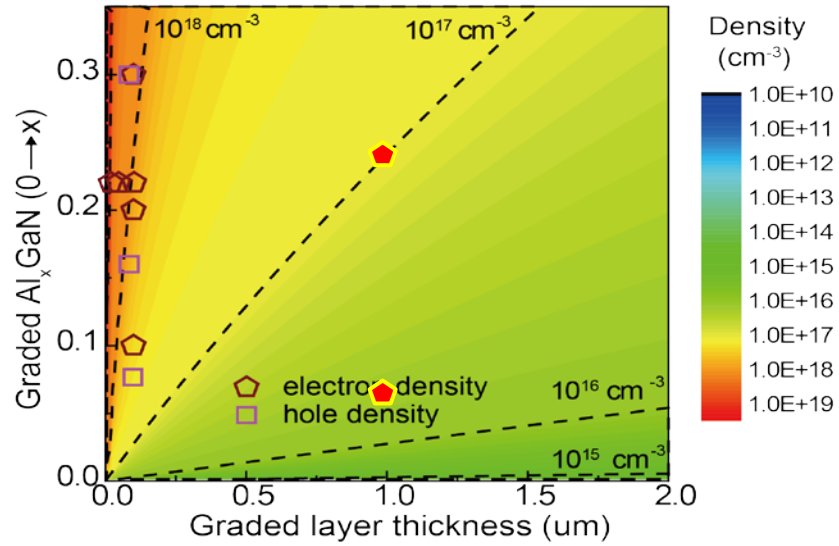


Figure 1.9 Charge density as a function of Al composition (x_{Al}) and graded-layer thickness (d). The reported experimental data are also included showing that there is a wide open range to explore below 10^{17} cm^{-3} , which is attractive for power switching applications [36].

1.3 Motivation and Outline of This Work

In this work, GaN based devices featuring polarization-enabled 2DEGs at heterojunction interfaces, 3DEGs and 3DHGs in bulk layers are studied for high-speed RF applications and high-voltage power switching applications.

In chapter 2, the ultimate limitations on the speed of GaN HEMTs with T-gates have been investigated for the high-speed RF application. The extrinsic delay is found to be a significant factor in limiting the speed in ultra-scaled GaN HEMTs, and is fundamentally determined by the device intrinsic g_m and the fringing capacitance between the gate stem and the access regions. Approaches to address this issue are also suggested.

In chapter 3, AlGaIn/GaN HEMTs on Si with non-alloyed regrown ohmic contacts and alloyed contacts are compared. Devices with non-alloyed regrown ohmic contacts feature a record-low leakage current, about six orders of magnitude smaller than that of the conventional devices with alloyed ohmics. Meanwhile, they also process a minimum current dispersion compared to devices with alloyed contacts.

In chapter 4, polarization-induced bulk-doping by linearly grading the Al composition in AlGaIn to form n-type and p-type layers has been integrated into design of GaN power devices. An analytical study was carried out to compare the traditional impurity-doped (imp-doped) GaN power devices and novel polarization-doped (Pi-doped) GaN power devices. High breakdown voltages ($BV > 1.2$ kV) have been experimentally demonstrated in both imp-doped and Pi-doped GaN vertical diodes. The vertical GaN p-n diodes have the desired avalanche breakdown capability and an ultra-fast reverse-recovery time, which make them very suitable for high-speed power switching.

In chapter 5, a lateral polar super junction (LPSJ) featuring charge balanced n/p-pillars by epitaxially grown graded AlGaIn layers has been proposed to break the traditional unipolar limit of GaN power devices. A 2D analytical modeling result of

the breakdown voltage (BV) and specific on-resistance $R_{on,sp}$ of GaN LPSJs under the charge balanced condition has been presented. Design examples at various x_{Al} composition values, together with the resulting BV and minimum $R_{on,sp}$, have been discussed. Furthermore, the adverse effects of charge imbalance on reducing the breakdown voltage of the devices are also modeled.

In Chapter 6, conclusions are drawn and the future works are proposed.

CHAPTER 2

EFFECT OF FRINGING CAPACITANCES ON THE RF PERFORMANCE OF GAN HEMTS WITH T-GATES

2.1 Introduction

High saturation velocity and breakdown electric field make GaN-based high electron mobility transistors (HEMTs) attractive for high-speed, high-power applications. Moreover, monolithically integrating enhancement-mode (E-mode) and depletion-mode (D-mode) devices can offer advantages such as fail-safe operation for power switches [37], straightforward implementation of direct coupled logic, and thus attractive for mixed signal applications [11]. Impressive progress has been made on both high-speed GaN HEMTs [1], [6], [7], [17], [19], [38], [39] and E/D-mode integration using either selective-area epitaxial regrowth [40] or gate recess [10], [41]. To date, high current-gain/power-gain cutoff frequencies (f_T/f_{max}) have been achieved primarily by an aggressive gate length scaling, assisted by a channel depth scaling through design of back barriers. In practice, when the gate length is reduced below 100 nm, the parasitic RC charging delay caused by source/drain (S/D) resistances and gate extrinsic capacitances can account for a significant fraction of the total delay [42]. This issue has been addressed by employing top barriers such as InAlN [6], [17] and InAlGaN [43] for high charge densities (thereby reducing the access resistance), regrown n^+ GaN contacts for ultralow contact resistances [1], [6], [7], [17], gate stems with high aspect ratios to reduce extrinsic capacitances due to the T-gate cap [1], [19],

and ultra-thin passivation to reduce extrinsic capacitances [14], [44]–[47][48]. The effect of the gate extrinsic capacitance on the RF performance of InP-based HEMTs has been widely reported [49], [50]; similar effects were also reported for rectangular gate GaN HEMTs [38]. However, these effects in the context of T-gate GaN HEMTs have not yet been carefully analyzed. The extrinsic capacitance associated with a T-gate can be divided into two components: parallel plate capacitances between the T-gate and the surrounding electrodes and the fringing capacitance between the gate stem and the access regions.

In this chapter, the impact of fringing capacitances on the high-frequency performance of GaN HEMTs with T-gates is investigated. The devices analyzed are InAlN HEMTs with a total gate length of 40 nm and f_T/f_{max} around 225/250 GHz [41]. Careful analysis of the measured results, in conjunction with numerical simulation of the capacitances shows that the extrinsic capacitance associated with the gate accounts for more than 40% of the total gate capacitance in these HEMTs for gate lengths in the range of tens of nanometers. This results in an appreciable parasitic delay that limits the speed of these highly scaled devices. Based on this analysis, simulations with optimized electrode geometries indicate that f_T of these HEMTs with a total gate length of 40 nm could increase from 225 GHz to ~270 GHz using an otherwise identical process flow; while if the process were changed to reduce R_c by 50% the f_T could increase to ~285 GHz assuming the same intrinsic g_m (~1.68 S/mm); furthermore, with negligible short channel effects (SCEs) and negligible channel mobility degradation due to gate recess thus a higher g_m , the HEMT f_T can further reach 370 GHz.

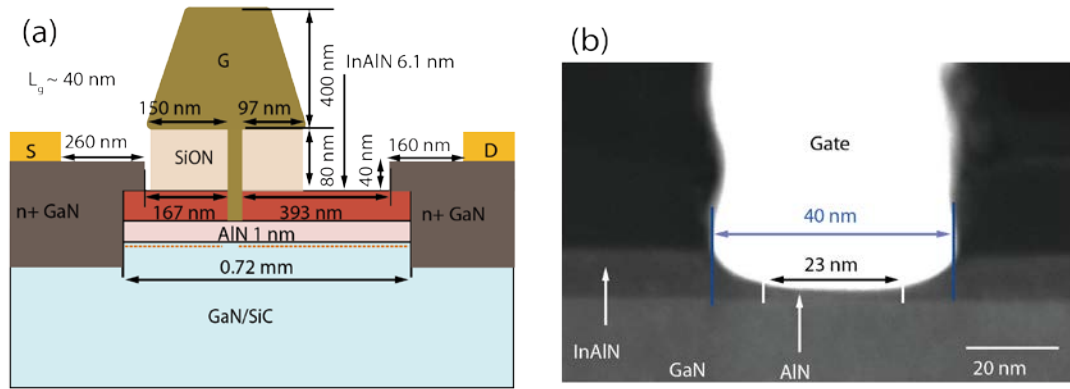


Figure 2.1 (a) Schematic of the T-gate HEMTs with recessed InAlN top barrier and (b) high resolution (HR) STEM image confirming the total L_g to be 40 nm [11]. (TEM taken by Faiza Faria)

More importantly, however, it is shown that the extrinsic capacitance of a planar HEMT is ultimately limited by the fringing capacitance between the gate stem and the access regions, which is “intrinsic” to the device layout and thus cannot be eliminated. This “intrinsic” extrinsic capacitance helps illustrate why it is challenging to achieve $> 500 \text{ GHz } f_T/f_{max}$ in GaN HEMTs.

2.2 Experiments

The $\text{In}_{0.17}\text{Al}_{0.83}\text{N}/\text{AlN}/\text{GaN}$ HEMTs analyzed in this work have an epitaxial structure consisting of a 6.1 nm InAlN barrier, a 1.0 nm AlN spacer, a 200 nm unintentionally-doped (UID) GaN channel, and a 1.6 μm Fe doped GaN buffer, which was grown by metal organic chemical vapor deposition (MOCVD) on a SiC substrate. A schematic cross section of the fabricated InAlN HEMT with recessed gate is shown in Fig. 2.1 along with a scanning transmission electron microscopy (STEM) image showing the gate foot geometry and dimensions.

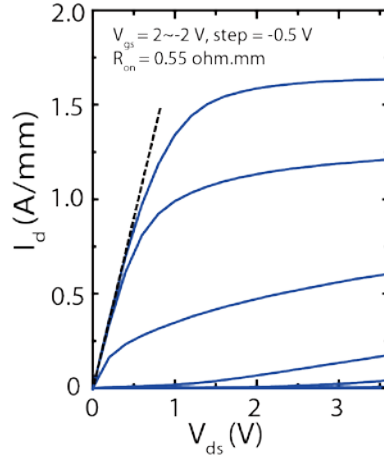


Figure 2.2 Common-source characteristics of the InAlN HEMT [11].

The devices were processed at TriQuint, using graded n^+ InGaN/GaN regrown ohmic contacts [51] and a dielectric etch-back process to remove part of the SiON dielectric around the T-gate. The resultant T-gate profile is shown schematically in Figure 2.1(a). The gate recess etch process is the same as reported in Ref. [52]. The total gate length L_g is ~ 40 nm, of which approximately 23 nm lies along on the bottom of the recessed region, flanked by two rounded, partially-recessed areas (Arc-shaped gate stem) (Fig. 2.1(b)). The gate width is $2 \times 25 \mu\text{m}$ and the source-drain distance L_{sd} is $\sim 0.72 \mu\text{m}$. Transmission line method (TLM) measurements yielded contact resistance R_c and sheet resistance R_{sh} of $0.13 \Omega \cdot \text{mm}$ and $310 \Omega/\square$, respectively.

2.3 Results and Discussions

The common-source characteristics of the HEMT are shown in Fig. 2.2. The HEMT exhibits a high current density of 1.6 A/mm at $V_{gs} = 2 \text{ V}$, $V_{ds} = 3.6 \text{ V}$ and a low on resistance of $0.55 \Omega \cdot \text{mm}$, attributed to the low contact resistance and small source-drain spacing (L_{sd}). Figure 2.3(a) shows the transfer characteristics, sweeping V_{gs} from

0 to 2 V; the peak extrinsic transconductance is 1306 mS/mm at $I_d \sim 0.7$ A/mm. Semi-log scale transfer curves at $V_{ds} = 0.1$ and 2 V are shown in Fig. 2.3(b). A drain-

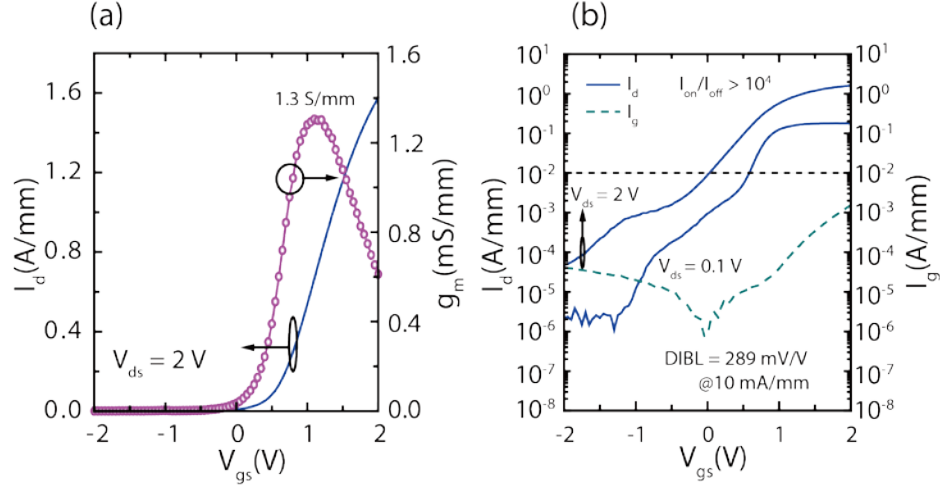


Figure 2.3 Transfer characteristics of the InAlN/AlN/GaN HEMT in (a) linear scale, showing the I_d and g_m versus V_{gs} at $V_{ds} = 2$ V and (b) logarithmic scale of I_d versus V_{gs} at $V_{ds} = 2$ V and $V_{ds} = 0.1$ V. The $DIBL$ extracted from the I_d at 10 mA/mm is 289 mV/V, which indicates strong short channel effects [41].

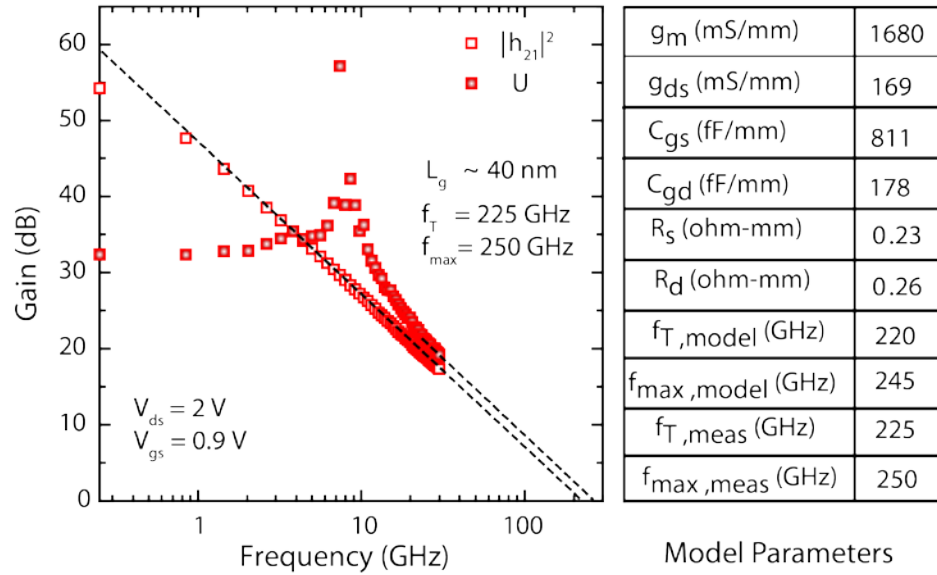


Figure 2.4 Small signal RF characteristics of the InAlN/AlN/GaN HEMT showing f_T of 225 GHz, f_{max} of 250 GHz, and table of extracted equivalent circuit parameters [41].

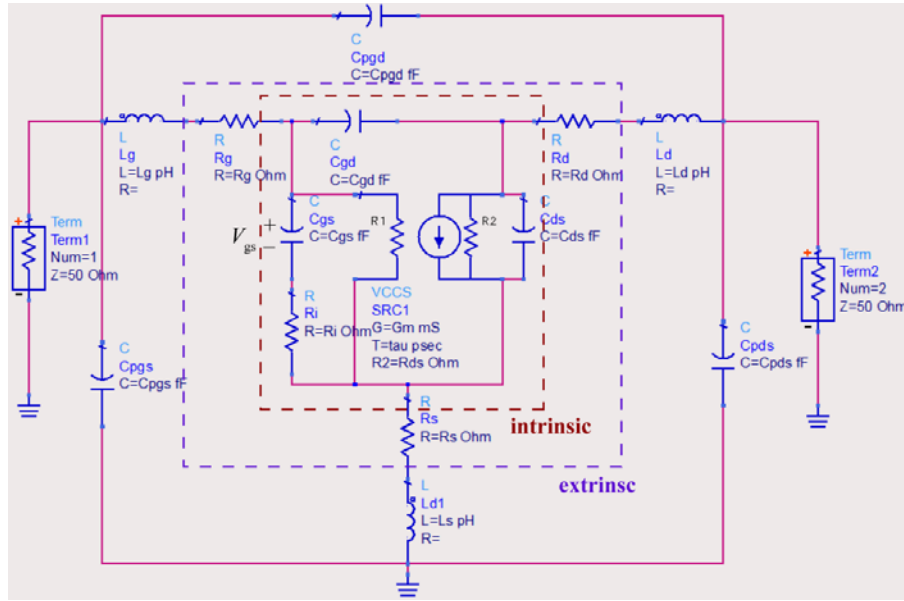
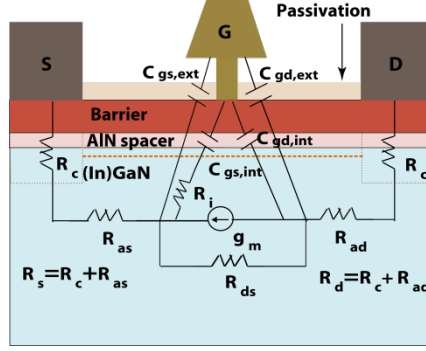


Figure 2.5 A representative HEMT with small signal equivalent circuit and the model implement in ADS [53].

induced barrier lowering of 289 mV/V extracted at a drain current of 10 mA/mm, indicating significant short channel effects. On-wafer RF measurements were taken using an Agilent 8510 vector network analyzer in the frequency range from 250 MHz to 30 GHz at bias conditions for peak f_T , $V_{ds} = 2$ V and $V_{gs} = 0.9$ V. Calibration was performed using LRM off-wafer impedance standards. The extrapolation of both $|h_{21}|^2$ and U with a -20 dB/dec slope gives f_T/f_{max} of 225/250 GHz after de-embedding with on-wafer open and short test structures as shown in Fig. 2.4. Small signal equivalent

circuit model shown in Fig. 2.5 was used to extract the device model parameters for better understanding device performance. The equivalent circuit parameters (ECP) shown in Fig. 2.4 are extracted from a good matching of measured and simulated *s-parameters* from 250 MHz to 30 GHz (Fig. 2.6).

Delay time analysis was performed following the method of Sensale-Rodriguez *et al.*[42], which is more suitable for field effect transistors with modest channel mobilities and a modification of the methods originally proposal by Moll *et. al.* [54] and Suemitsu [55]. This method consists of two de-embedding steps: 1) de-embedding the probe pads' reactive effects – a standard procedure to measure the device speed f_T or the total delay $\tau_{total}=1/(2\pi f_T)$, 2) de-embedding the parasitic resistance (R_s+R_d) and extrinsic gate-source and gate-drain capacitances ($C_{gs,ext}$ and $C_{gd,ext}$) using the coldFET measurement. After the second de-embedding, the extracted device delay is the total intrinsic device delay– comprised of the intrinsic gate delay

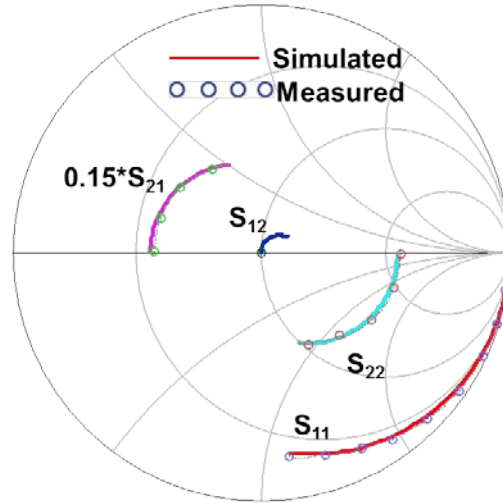


Figure 2.6 Simulated and measured *s-parameters* from 250 MHz to 30 GHz.

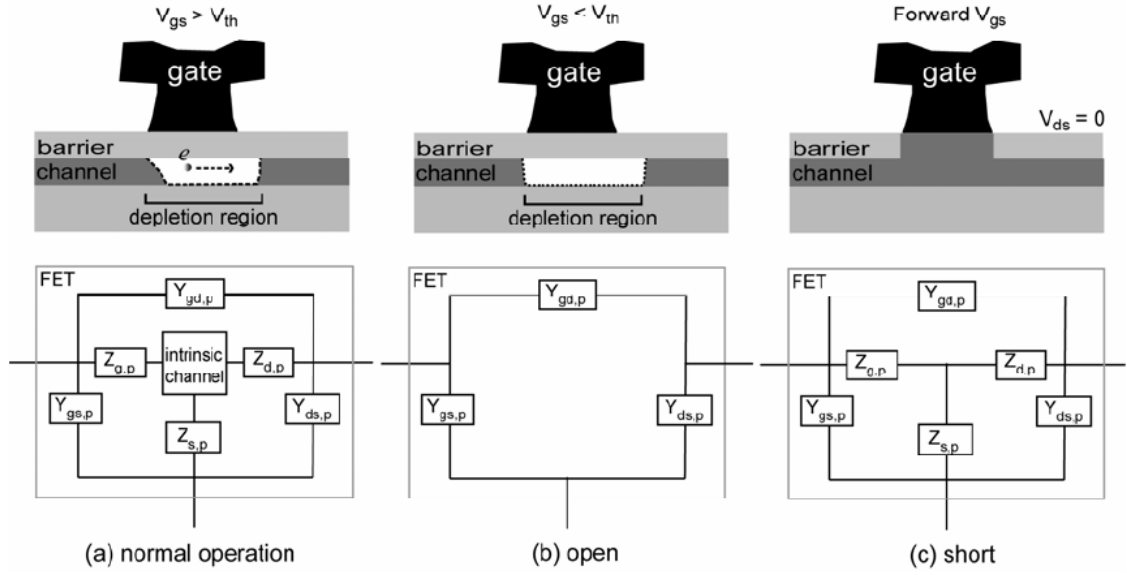


Figure 2.7 (a) Parasitic elements in the device after deembedding the effect of the probe pads, the impedances (Z 's) represent the devices access parasitic resistances while the admittances (Y 's) represent the extrinsic parasitic capacitances. (b) Equivalent circuit model where $V_{gs} < V_{th}$ and device's channel is depleted below the gate region thus only the extrinsic parasitic capacitances are present. (c) Equivalent circuit model when $V_{gs} > V_{th}$ and $V_{ds} = 0$ V; the intrinsic device behaves as short. From the S parameters under the bias conditions depicted in (a–c), we can deembed the effects of these extrinsic parasitic resistances and capacitances thus obtaining the intrinsic device speed information [42].

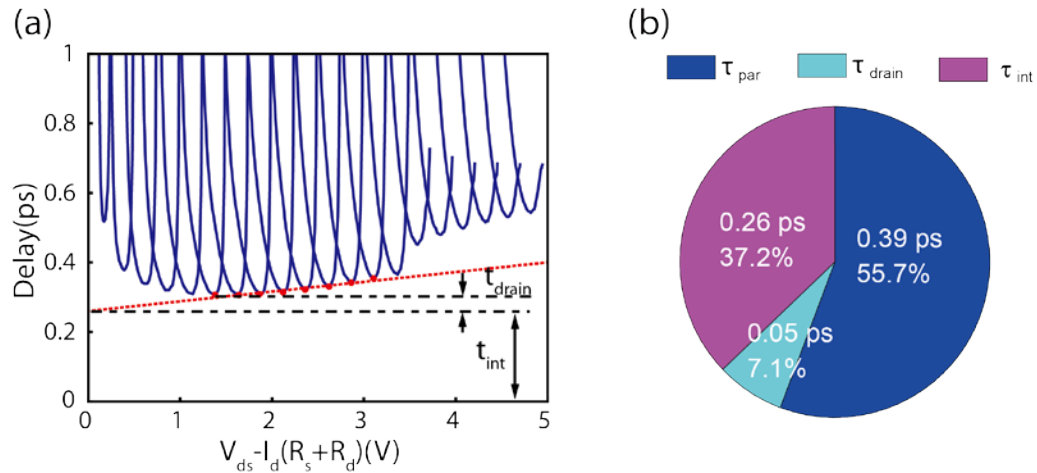


Figure 2.8 (a) Delay analysis of the E-mode HEMT for extraction of the intrinsic delay and drain delay using the two-step deembedding method (the modified Suemitsu method) and (b) Delay time analysis results showing that the parasitic delay stemming from extrinsic components accounts for more than half of the total delay [11].

τ_{int} and the drain delay τ_d . Subsequently, the parasitic delay time τ_{par} is computed by subtracting the total intrinsic device delay from the total delay, i.e. $\tau_{par} = \tau_{total} - \tau_{int} - \tau_d$. For the device analyzed here (Fig. 2.1), the resultant delay time components are $\tau_{total} = 0.7$ ps, $\tau_{int} = 0.26$ ps, $\tau_d = 0.05$ ps and $\tau_{par} = 0.39$ ps, respectively. From this analysis, it can be seen that in these devices the delay associated with charging the extrinsic capacitances accounts for more than 50% of the total delay time.

To gain insight into the physical origin of the significant parasitic delay, careful analysis and modeling of the parasitics (i.e. extrinsic components) is needed. From the analytic expression for f_T [50], the total parasitic delay can be expressed as:

$$\tau_{par} = (C_{gs,ext} + C_{gd,ext})/g_m + C_{gd}(R_s + R_d) + (C_{gs} + C_{gd})(R_s + R_d)g_{ds}/g_m \quad (2.1)$$

where $C_{gs,ext}$ is the extrinsic gate-source capacitance, $C_{gd,ext}$ is the extrinsic gate-drain capacitance, and g_m is the intrinsic transconductance, i.e. $g_{m,int}$. Based on the ECP values, the third term in Eq. (2.1), $(C_{gs} + C_{gd})(R_s + R_d)g_{ds}/g_m$, is 0.05 ps, describing delay due to the SCEs. The second term, $C_{gd}(R_s + R_d)$, has a value of 0.09 ps, which corresponds to about one quarter of the total parasitic delay. Therefore, the dominant parasitic delay in this device is the first term, $(C_{gs,ext} + C_{gd,ext})/g_m$, which describes the delay due to charging of the extrinsic gate capacitance. This analysis depends critically on accurate values and correct partitioning of the intrinsic and extrinsic capacitances. To verify that the capacitances are accurate, the extrinsic capacitances have been extracted from two independent methods: electrostatic simulations using COMSOL, and analysis of the *s-parameters* from on-wafer ColdFET measurements.

As will be shown, the good agreement between these two methods confirms that the dominant parasitic delay is associated with the extrinsic gate capacitance.

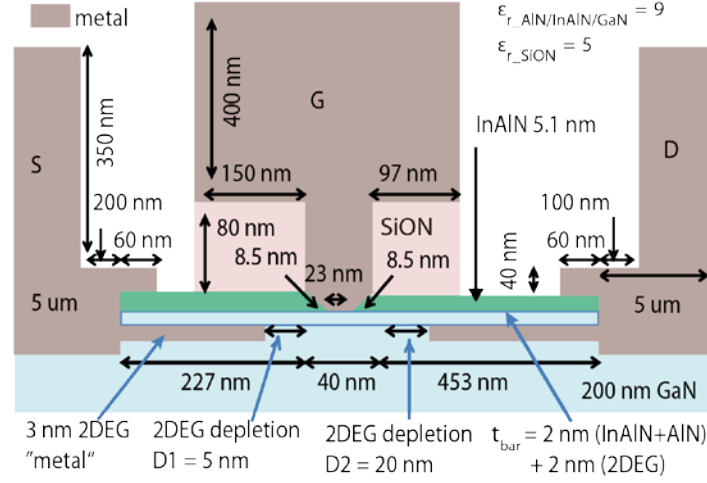


Figure 2.9 COMSOL simulation setup based on the geometries obtained from the TEM image in Figure. 1b and the 2DEG lateral depletion widths obtained from TCAD simulations [11].

The geometry used in COMSOL simulations is shown in Figure 2.9, largely based on the TEM image in Figure 2.1. In order to model the 2DEG's lateral distribution, numerical TCAD simulations were performed to estimate the 2DEG lateral depletion in the channel under the ColdFET bias condition of $V_{gs} = -4$ V and $V_d = 2$ V used in the delay analysis; extensions of about 5 and 20 nm towards the source and drain were found, respectively. The undepleted 2DEG access regions are modeled as perfect conductors connected to the source and drain contacts, while the depleted region is treated as an insulating region. The barrier thickness t_{bar} under the gate is taken to be 4 nm, which consists of ~1 nm remaining InAlN, 1 nm AlN and 2 nm GaN representing the separation of the 2DEG centroid from the AlN/GaN surface. The SiON relative permittivity ϵ_r is assumed to be 5 and the relative permittivity ϵ_r of AlN, InAlN and

GaN layers are all assumed to be 9. The extrinsic capacitance is extracted from the simulations using the following procedure: 1) the surface charges at the source contact and the drain contact are summed up separately (including the charge in the 2DEG access regions), 2) the charge associated with the source is divided by the voltage difference between the gate and source to get $C_{gs,ext}$; an analogous approach is used with the drain contact to obtain $C_{gd,ext}$. The extrinsic capacitances $C_{gs,ext}/C_{gd,ext}$ were thus estimated from these simulations to be $\sim 260/162$ fF/mm, respectively.

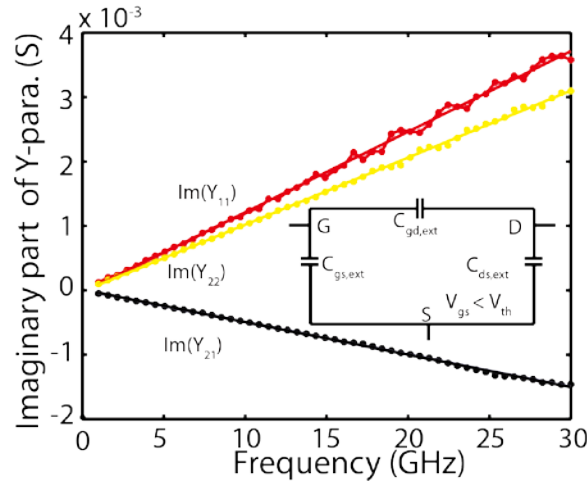


Figure 2.10 Measured Y parameters of the HEMT under the ColdFET bias condition with frequency ranging from 250 MHz - 30 GHz. The extrinsic capacitance can be extracted from the slope of the Y -parameters. Inset: equivalent circuit model of the HEMT when $V_{gs} < V_{th}$, where only the extrinsic capacitances are present since channel is fully depleted [11].

The extrinsic capacitances were also extracted from measured s -parameters under ColdFET bias conditions, where the HEMT can be modeled as three capacitors between the source, gate and drain terminals (inset of Figure 2.10) since the channel is depleted under this bias. $C_{gs,ext}$ and $C_{gd,ext}$ can then be extracted using the following equations [56]:

$$Im(Y_{11}) = \omega(C_{gs,ext} + C_{gd,ext}) \quad (2.2)$$

$$\text{Im}(Y_{22}) = \omega(C_{ds,ext} + C_{gd,ext}) \quad (2.3)$$

$$\text{Im}(Y_{12}) = \text{Im}(Y_{21}) = -\omega C_{gd,ext} \quad (2.4)$$

In Fig. 2.10, the measured Y parameters are plotted as a function of frequency. Linear fits to the slopes in Fig. 2.10 were found to result in $C_{gs,ext}/C_{gd,ext}$ of 238/161 fF/mm, respectively, in good agreement with the values of 260/162 fF/mm obtained from COMSOL simulations.

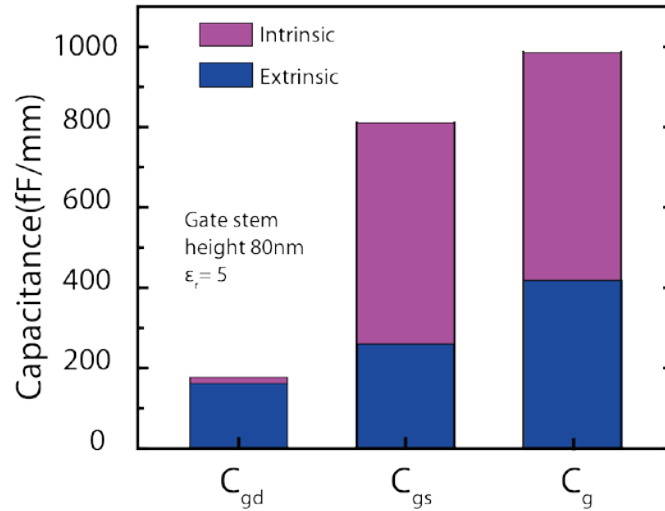


Figure 2.11 Extrinsic capacitances (extracted from COMSOL) and intrinsic capacitances (were obtained by subtracting the COMSOL extrinsic capacitances from the ECP C_{gs} and C_{gd} values); the extrinsic capacitance is approximately 40% of the total gate capacitance.

Assuming that the *extrinsic* capacitances under the peak f_T bias condition ($V_{gs} = 0.9$ V and $V_d = 2$ V) are the same as those under the ColdFET bias condition, the intrinsic capacitances can be estimated by subtracting the extrinsic capacitances from the ECP C_{gs} and C_{gd} values obtained from measurements. The calculated intrinsic capacitances for the HEMT analyzed here are shown in Fig. 2.11. It is worth noting that this assumption of constant extrinsic capacitance with bias slightly underestimates C_{ext}

since the 2DEG depletion extensions are shorter under the peak f_T bias than under the ColdFET bias conditions. Nevertheless, the extrinsic capacitances are found to account for approximately 40% of the total gate capacitance. This extrinsic capacitance yields a total parasitic delay time of ~0.37-0.39 ps, in close agreement with the delay time analysis (0.39 ps) shown in Fig.2.8.

2.4 Optimization of the Extrinsic Capacitance

The substantial parasitic delay limits the improvement in f_T that can be achieved by further gate length scaling; further increases in device speed require reduction in these parasitic capacitances. Reduction of extrinsic capacitance can be achieved by raising the T-gate stem height, dielectric etch-back, ultrathin passivation schemes [45], and even eliminating the T-gate cap. The effectiveness of each of these approaches is discussed below.

The T-gate cap forms a parallel plate capacitance with the access regions. When the T-gate cap is raised further away from the channel, this parasitic capacitance should decrease. The key question is how large of a spacing is sufficient to maximize performance. To address this, COMSOL simulations based on the geometry shown in Fig. 2.9 were performed, but with key geometric parameters adjusted to show the trends. As shown in Fig. 2,12a&b, the total fringing capacitances $C_{gs,ext}/C_{gd,ext}$ (with SiON) can be lowered to 231/150 fF/mm from 260/162 fF/mm if the gate stem and dielectric under gate cap height increases from 80 nm to 200nm while keeping the rest of the device geometry the same. Increasing the gate stem to 300 nm does not result in any significant further reduction in capacitance. When the dielectric surrounding the gate is completely removed, the extrinsic capacitances can be reduced from 231/150

fF/mm to ~160/101 fF/mm for a gate stem height of 200 nm. The extrinsic capacitances with (solid lines) and without (dash lines) a T-gate cap are also compared in Fig. 2.12(a) and (b). It can be seen that the parasitic capacitances $C_{gs,ext}/C_{gd,ext}$ associated the gate stem increase with increasing gate stem height, while the parasitic capacitance associated with the T-gate cap decreases. Beyond a gate stem height of 200 nm, the parasitic capacitance is completely dominated by the capacitance due to the gate stem alone. The small difference in $C_{gs,ext}/C_{gd,ext}$ between the solid and dashed lines, ~15 fF/mm at a gate stem of 300 nm, arises from the parasitic capacitance between the gate cap and the ohmic metal. Meanwhile, the angle of the stem sidewall would also affect the fringing capacitance. The simulation suggests the rectangular gate stem would lead to a higher extrinsic fringing capacitance than the arc-shaped gate stem due to stronger field coupling between the two sharp edges at the gate stem and the 2DEG metal. On the other hand, the optimization discussed here has the similar effect on the rectangular gate stem device.

This analysis also suggests that the speed improvement observed in previously reported “I-gate” devices is largely due to the low parasitic capacitances associated with the short gate stem and without T-cap (< 50 nm) [6], [7], [17]. However, as is well-known, I-gate devices have poor f_{max} due to high gate resistance. This analysis shows that as the gate stem height is increased (to lower the gate resistance and improve f_{max}), the advantage of the I-gate rapidly diminishes. The importance of low- k passivation is also apparent since the parasitic capacitance can be lowered by ~30% by eliminating the dielectric surrounding the gate.

Based on this analysis, simulations with optimized electrode geometries (a gate stem height of 200 nm and a gate-cap ohmic-post distance over 1.5 μm) indicate that f_T of the HEMT shown in Figure 2.1 with a total gate length of 40 nm could increase from 225 GHz to ~270 GHz using an otherwise identical process flow, while if the process were changed to further reduce R_c by 50% the f_T could increase to ~285 GHz assuming the same intrinsic g_m (~1.68 S/mm).

2.5 Effect of Gate Recess

The lower bound on the extrinsic capacitance is established by the fringing electric field between the gate stem and the device access regions (Fig. 2.12 (c)). However, to enhance device transconductance g_m and shift threshold voltage, a gate recess process is commonly used. As the top barrier is recessed, the gate becomes closer to the access regions, and is also surrounded by the remaining semiconductor barrier with its relatively high permittivity; as a result, this lower bound for the gate fringing capacitance is expected to be higher for a recessed device compared to a device with the gate on the semiconductor surface. For example, in a conventional AlGaIn/GaN HEMT the top AlGaIn barrier is typically ~30 nm thick and the remaining barrier after gate recess is ~10 nm; even without considering the dielectric passivation, the gate fringing capacitance from the recess can be significant due to the semiconductor surrounding the gate stem near the foot. In InAlN HEMTs, the InAlN barrier is generally thin (<10 nm).

To illustrate the effect of gate recess on device speed, the calculated extrinsic capacitance for InAlN HEMTs with thin (6 nm) and thick (30 nm) top barriers and a series of recess depth under the gate are compared. In the COMSOL simulations, a

gate stem height of 200 nm was used; all of the other parameters remain the same as in Fig. 2.9. For these simulations, the same 2DEG lateral depletion was used since the channel 2DEG concentration is nearly the same for an InAlN barrier thickness higher

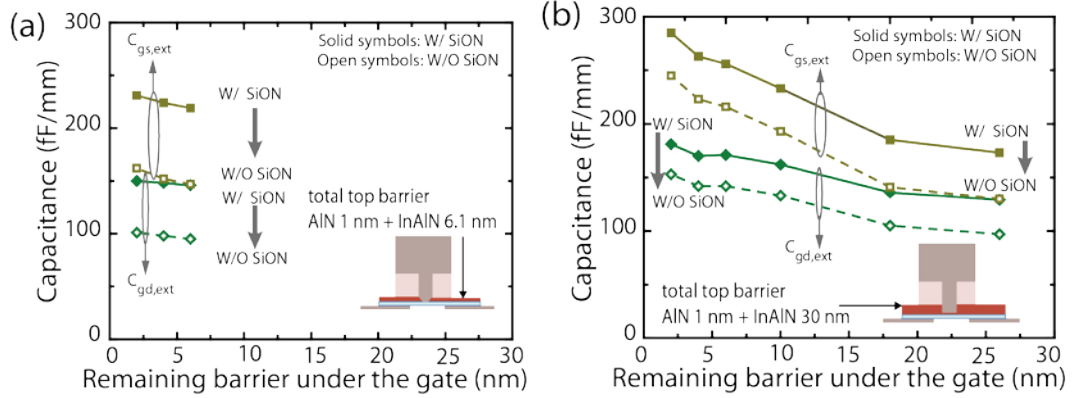


Figure 2.13 Simulated extrinsic capacitances with a gate stem height of 200 nm as a function of the remaining barrier thickness under the recessed gate for HEMTs with (a) a 6 nm total barrier, and (b) a 30 nm total barrier. The insets show the geometry used in the COMSOL simulations [11].

than 5 nm, and the peak f_T typically occurs near the same 2DEG concentration under the gate [57]. The results are shown in Fig. 2.13. In addition, the capacitances with and without SiON passivation under the gate cap are included for comparison. In all cases, $C_{gs,ext}$ and $C_{gd,ext}$ increase with increasing recess depth (decreasing residual barrier thickness under the gate), as expected. The key observation is that $C_{gs,ext}$ and $C_{gd,ext}$ are smaller for the same remaining barrier thicknesses in the thin-barrier HEMTs in comparison to the thick barrier HEMTs. The thin-barrier HEMTs also show a more constant $C_{gs,ext}$ and $C_{gd,ext}$. These effects originate from the fact that the dielectric constant of the passivation has been assumed to be lower than that of the semiconductor. In addition, the extrinsic capacitance associated with the fringing field between the gate stem and the access regions is independent of the gate length (not

shown). As a result, it is possible to experimentally extract the extrinsic capacitances by plotting the total gate capacitance versus the gate length, provided the SCEs do not significantly influence the extraction of the gate capacitance[38].

2.6 Performance Projection

With C_{ext} , g_m , R_s and R_d , one can calculate the expected f_T while neglecting the SCEs. According to Ref. [57], g_m can be expressed as:

$$g_m = (\partial J / \partial n_{s,0}) C_{gs,int} \quad (2.5)$$

$$v_{eff} = \partial J / \partial n_{s,0} \quad (2.6)$$

where $n_{s,0}$ is the 2DEG density at the source, v_{eff} is the effective injection velocity, $C_{gs,int}$ is the intrinsic gate capacitance. $C_{gs,int}$ can be obtained from 1D self-consistent Schrodinger-Poisson simulations for different remaining barrier thicknesses after gate recess. The results are shown in Fig. 2.14 for the 6.1 nm InAlN barrier case considered in Fig. 2. 13 (a), assuming a v_{eff} of 1.5×10^7 cm/s[57]. Since both $C_{gs,int}$ and g_m scale inversely with the remaining recessed barrier thickness, the intrinsic delay is independent of recess depth. On the other hand, the parasitic delay due to extrinsic capacitance decreases as the remaining barrier thickness is reduced since g_m increases while the parasitic capacitances depend only weakly on recess etch depth (Fig. 2. 14 (a)). Thus, the device speed increases with decreasing remaining barrier thickness, i.e. more aggressive gate recess, provided the v_{eff} is not affected by the recess etch.

To predict the degree of improvement in f_T expected for the HEMTs shown in Fig.2.1 using the otherwise same device parameters but with a v_{eff} of 1.5×10^7 cm/s, optimized gate stem height and contact resistance, lower values of $R_s/R_d=0.11/0.18 \Omega$ -

mm [6], among the best reported in the literature, were used in Fig. 2.14 (d). It is found that for the optimized 40 nm device, f_T about 370 GHz can be achieved, which is close to the best reported GaN HEMT device with T-gate [1], [10]. Since the intrinsic $C_{gs,int}$ scales with gate length, i.e. the intrinsic capacitance of the 20 nm gate length device is half that of the 40 nm device, the projected speed performance of a 20 nm device (Fig. 2.14 (d)) can potentially reach 500 GHz with low-k passivation.

It should be noted that although InAlN barrier HEMTs have been used for the analysis presented here, this analysis applies more generally to all planar HEMTs independent of material system, since *the fringing capacitance between the gate stem and access region, together with g_m , ultimately limits the device speed even when the contact resistance is optimized to be zero and the electrodes are far from the gate.* Therefore, this study suggests that maximizing g_m is the key to obtaining terahertz transistors. This is consistent with observations that InGaAs-channel HEMTs exhibit higher speed than GaN or Si based FETs. To further improve the GaN HEMT speed, it is paramount to seek approaches that enhance injection velocity thus g_m , such as the use of InGaN [58] or isotope-disordered channels [59].

Finally it is worth noting that SCEs have been explicitly neglected in this analysis; since AlGaIn [1] and InGaIn [17] back barriers have been widely employed, the mitigation of SCEs is well-understood and straightforward. Furthermore, one of the ultimate embodiments on SCE control is AlN/GaN/AlN quantum well HEMTs, which has been also recently demonstrated[60].

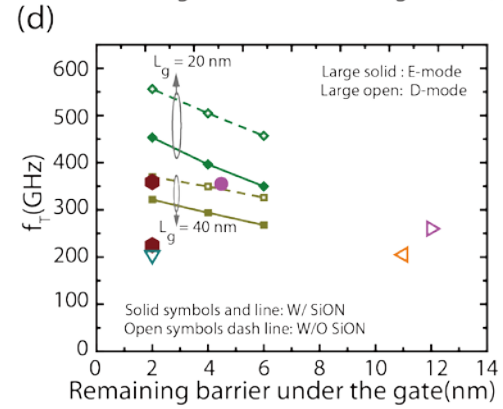
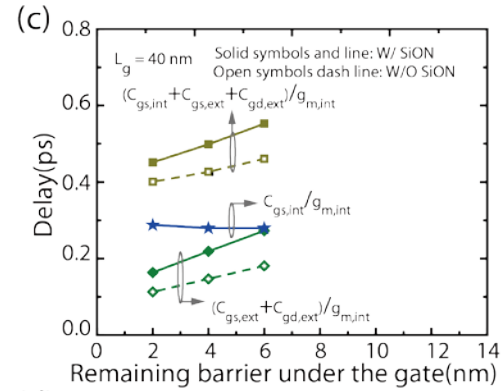
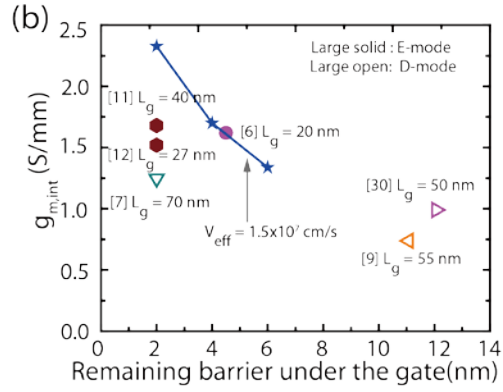
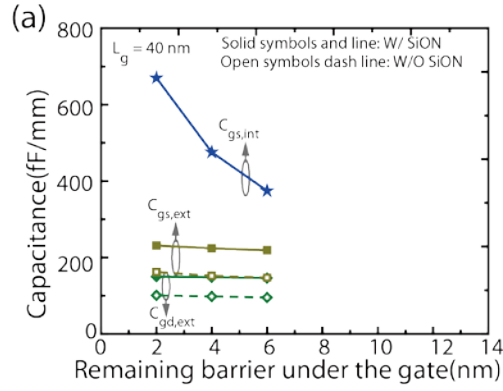


Figure 2.14 Calculated performance of GaN HEMTs with a gate stem height of 200 nm, recessed gate and a thin barrier shown in Fig. 6a. For a gate length of 40 nm, (a) extrinsic and intrinsic capacitances, (b) estimated intrinsic g_m and reported values, and (c) delays. The intrinsic delay stays the same (SECs neglected), the extrinsic delay decreases purely because of the enhancement in g_m . (d) Projected f_T for devices with R_s/R_d of 0.11/0.18 Ω .mm and two gate lengths: 20 and 40 nm. Also shown are f_i values of several reported high performance E-mode GaN HEMTs with T-gate (large solid symbols) [11].

2.7 Effect of Scaling of the Source-Drain Distance

In this section, the impact of source-drain distance scaling and its effect on gate fringing capacitance and the resulting impact on the high frequency performance of T-gate recessed InAlN HEMTs are investigated. We observe that scaling the source-drain distance reduces the parasitic resistance, but it also increases the fringing capacitance. Consequently, the speed of devices with un-scaled L_{sd} and that of devices with scaled L_{sd} become comparable due to this tradeoff in fringing capacitance.

The un-scaled device is the one just discussed aforementioned. The scaled devices have L_{sd} 's of $\sim 0.13 \mu\text{m}$ and L_g 's of $\sim 24 \text{ nm}$ as shown in Fig. 2. 15. A dielectric etch-back process was applied for the scaled devices to completely remove the dielectric under the T-gate cap to minimize parasitic capacitances.

The DC and small signal RF characteristics for a scaled- L_{sd} device are shown in Fig. 2.16. The device has a high current capability $\sim 3 \text{ A/mm}$ at $V_{gs} = 2.5 \text{ V}$ and $V_{ds} = 6 \text{ V}$ and a low on-resistance of 0.31 ohm.mm . Besides, it also has a high extrinsic transconductance of 1.21 S/mm at $V_{ds} = 2 \text{ V}$. The *s-parameter* measurements from 0.1 to 110 GHz are performed using an Agilent N5250C with the LRRM calibration using off-wafer impedance standards. Extraction of $|h_{21}|^2$ and U yield f_u/f_{max} of 339/328 GHz after de-embedding as shown in Fig. 2.16. From the delay time analysis, it was found

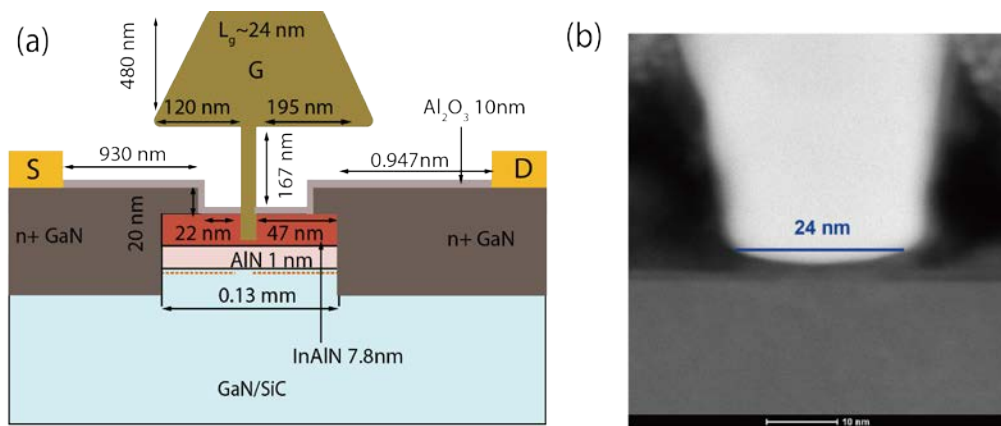


Figure 2.15 (a) Schematic of the gate recessed E-mode scaled InAlN HEMTs with L_{sd} ($\sim 0.13 \mu\text{m}$) and $L_g \sim 24 \text{ nm}$ and (b) high resolution (HR) STEM image confirming the total L_g to be 24 nm (TEM by Prof. Sergei Rouvimov).

that the parasitic delay for the un-scaled/scaled device is 0.39/0.28 ps respectively as shown in Fig. 2.17. This parasitic delay represents more than 50% of the total delay time for both devices. Equivalent circuit parameters (ECPs) extracted from on-wafer *s-parameter* measurements are shown in Table 2.1; from these ECPs and the equation 2.1, one can see that the dominant parasitic delay time originates from the extrinsic fringing capacitances $C_{gs,ext}$ and $C_{gd,ext}$. For the 24-nm HEMT device the extrinsic parasitic capacitances are higher due to the close spacing between the contacts (see Fig. 2.15); even with a gate stem ~ 170 nm tall and no dielectric under the gate, the fringing capacitance extracted from *S-parameters* is about 194/158 fF/mm, higher than 160/101 fF/mm in the 40-nm HMET device. The main reason may be attributed to the scaling of the source-drain distances. Since the gate-to-source distance and the gate-

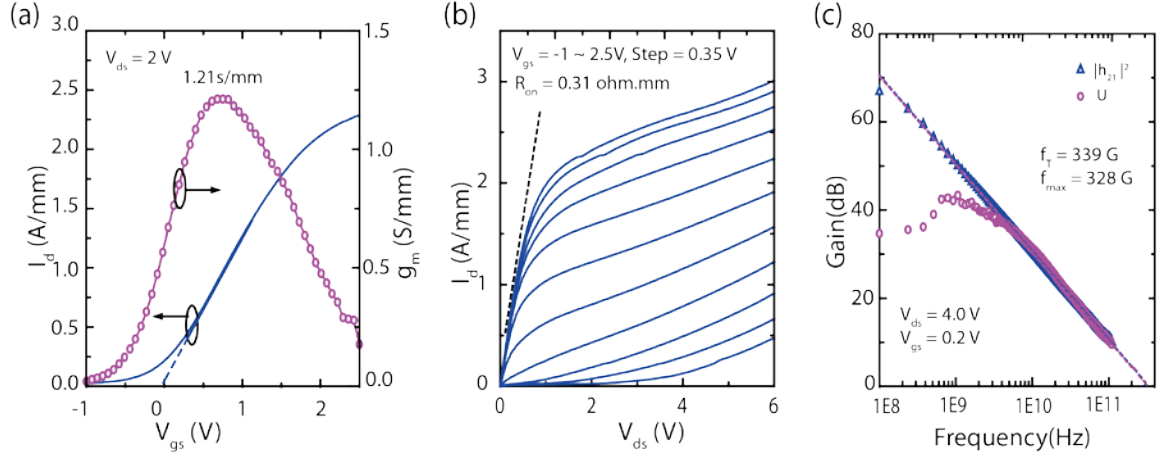


Figure 2.16 Characteristics of scaled devices shown in Fig. 2.15: (a) transfer characteristics, (b) common source I-Vs, and (c) on-wafer small signal performance.

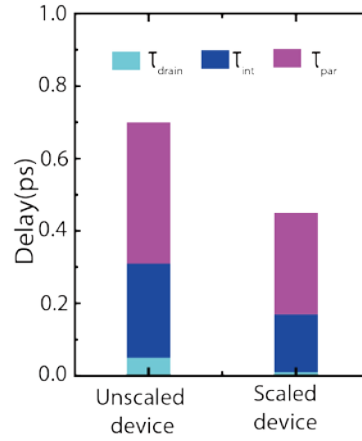
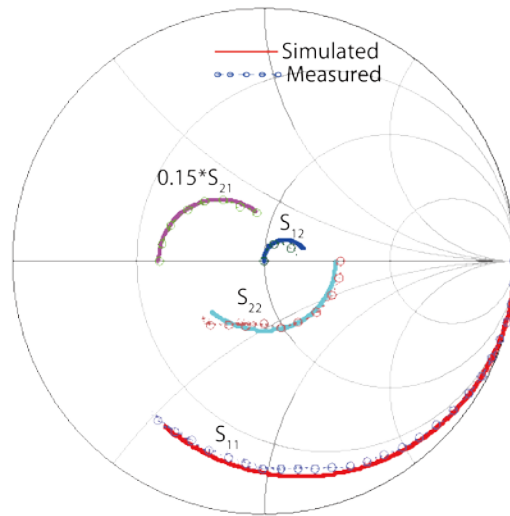


Figure 2.17 Comparison of the delay time in the device 40-nm HEMT (Fig. 2.1) and the device with scaled- L_{sd} and 24-nm HEMT (Fig. 2.15).

to-drain distance reduce, coupling between the gate and the regrown region increases, which in turn leads to a high fringing capacitance as shown in Fig. 2.19 though it helps to reduce R_s and R_d (see Table 2.1). Based on this understanding, we have estimated the speed of a device with unscaled- L_{sd} but with the gate length decreased from 40 nm to 24 nm and optimized fringing capacitances of 160/101 fF/mm. A f_T of 340 GHz is expected, which is comparable to that of the device with a scaled L_{sd} , ~ 339 GHz.



Frequency from 0.1 to 110 GHz

Figure 2.18 Simulated and measured *s*-parameters from 0.1 to 110 GHz.

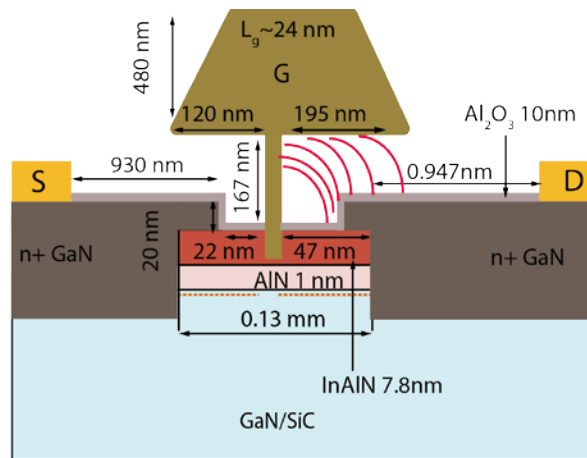


Figure 2.19 Sketch to highlight the fringing capacitance between the gate stem and ohmic region (red lines) due to the scaling of the source-to-drain distance.

This analysis provides new insight about the source-drain-distance scaling and highlights the significance of fringing capacitances in ultra-high speed HEMTs in general.

Table 2.1 Extracted equivalent circuit parameters of devices with unscaled and scaled source-drain distances.

	40-nm un-scaled [7]	24-nm scaled	24-nm un-scaled projected
g_m (mS/mm)	1680	1638	1638
g_{ds} (mS/mm)	169	276	276
C_{gs} (fF/mm)	811	494	490
C_{gd} (fF/mm)	178	160	111
R_s (Ω .mm)	0.23	0.10	0.23
R_d (Ω .mm)	0.26	0.20	0.26
f_T (GHz) ECP	220	332	340
f_{max} (GHz) ECP	245	326	277
f_T (GHz) meas.	225	339	-
f_{max} (GHz) meas.	250	328	-

2.8 Ultimate Limit of GaN HEMT Speed Toward THz Applications

When both L_g and L_{ds} are scaled down to sub-100 nm regime, the device speed is limited by the parasitic delay, mostly from the first term of Eq.2.1, associated with the extrinsic capacitance ($C_{gs,ext} + C_{gd,ext}$) and the intrinsic transconductance g_m of the transistor. The extrinsic capacitance depends on the device geometry and passivation dielectrics (both the thickness and dielectric constant) thus not scaling down with a decreasing L_g . As shown in Fig.2.12 (a) and (b), the extrinsic capacitance shows little dependence with the gate recess depth, while the intrinsic capacitance and g_m scale inversely with the remaining recessed barrier thickness. Thus, the intrinsic delay is independent of recess depth. On the other hand, the parasitic delay due to extrinsic capacitance decreases as the remaining barrier thickness is reduced since g_m increases. The device speed increases with a decreasing remaining barrier thickness, i.e. more

aggressive gate recess, provided the v_{eff} is not affected by the recess etch. **It is $(C_{gs,ext}+C_{gd,ext})/g_m$ that defines the ultimate speed limit after both L_g and R_{on} scale down to zero in theory.** Moreover, the limit of the fringing capacitance for a HEMT with a 2 nm remaining barrier thickness under the gate and assuming the 2DEG is about 2 nm from the barrier is explored in Fig. 2.20. It shows that even scaling gate length down to 4 nm, the fringing capacitance is still about 50 fF/mm in air ambient (see Fig. 2.20 (b)). Thus the delay time due to the limit of the fringing capacitance only as a function of the intrinsic g_m is shown in Fig. 2.19(c). The record speed experiment data are also included for comparison. It can be found that there is still space to improve g_m and lower fringing capacitances for pushing GaN HEMTs towards THz applications. Besides, it is also found that maximizing g_m is the key to obtaining terahertz transistors. This is consistent with the observation that InGaAs-channel HEMTs exhibit a higher speed than GaN or Si-based FETs shown in Fig.2.21. To further improve the GaN HEMT speed, it is paramount to seek approaches that enhance injection velocity thus g_m , such as the use of InGaN or isotope-disordered channels.

2.9 Conclusion

The ultimate limitations on the speed of GaN HEMTs with T-gates have been investigated. The extrinsic delay is found to be a significant factor in limiting the speed in GaN HEMTs, and is fundamentally determined by the device intrinsic g_m and the fringing capacitance between the gate stem and the access regions. This result is intrinsic to all FETs with planar geometry, therefore, $(C_{gs,fringing}+C_{gd,fringing})/g_m$ could be considered as an “inherent” delay in high frequency FETs since it can not be

eliminated by geometric optimization. The effect of gate recess on this fringing capacitance in HEMTs with thin and thick top barriers was also investigated. The intrinsic delay is found to be independent of gate recess depth, while the extrinsic delay is reduced for deeper recesses, due to the increase in g_m , so long as the channel injection velocity is not compromised. Therefore, improving g_m by enhancing injection velocity is key in realizing high speed FETs.

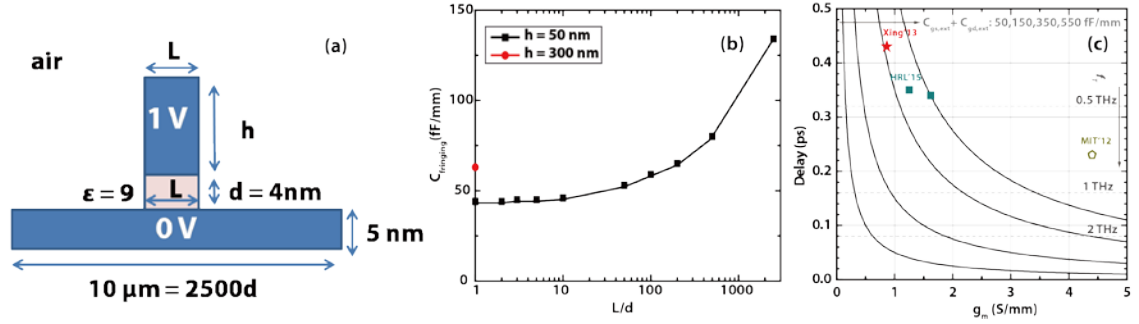


Figure 2.20 (a) Schematic of HEMT device structure to extract the fringing capacitance with 2 nm barrier remaining and assuming the centroid of 2DEG is about 2 nm far from the barrier therefore $d = 4 \text{ nm}$. (b) Extracted fringing capacitance verse gate length, (c) calculated delay time associated with the fringing capacitance only, which determines the ultimate limit of the speed of GaN HEMTs. Also shown are record-setting transistors experimentally demonstrated by various groups. Solid symbols are for GaN HEMTs and the hollow ones are for InGaAs-based HEMTs.

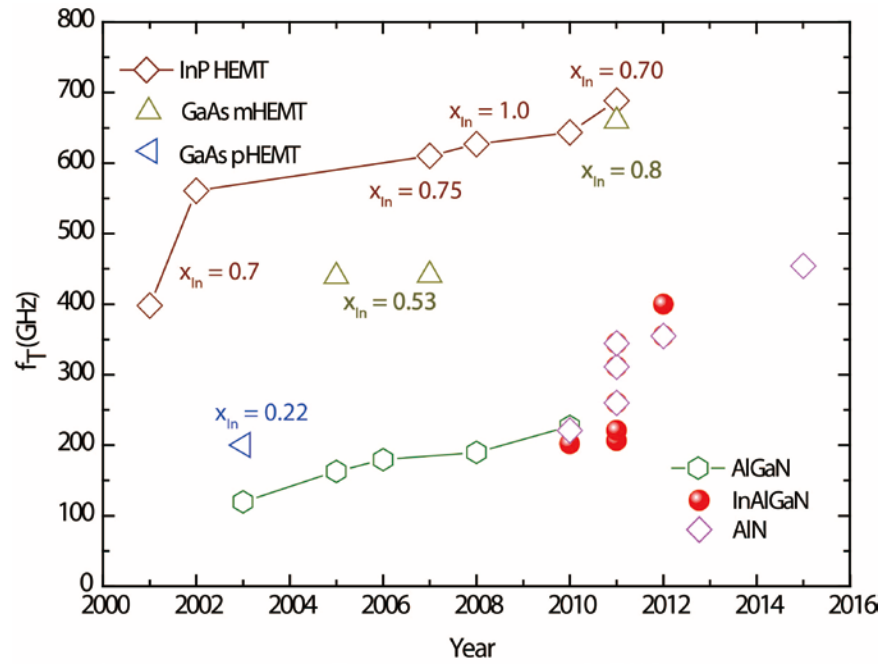


Figure 2.21 The evolution of f_T in the last one decade for both III-V pHEMTs and GaN HEMTs

CHAPTER 3

ULTRALOW-LEAKAGE ALGAN/GAN HIGH ELECTRON MOBILITY TRANSISTORS ON SI WITH NON-ALLOYED REGROWN OHMIC CONTACTS

3.1 Introduction

GaN based high electron mobility transistors (HEMTs) have demonstrated great potential for high-speed, high-power RF applications[6], [19] and next-generation power electronics [26], [61]. In addition, the adoption of a Si substrate would pave the way for low cost and high-performance GaN electronics. However, the high leakage current often observed in GaN HEMTs causes extra noise in power amplifiers[62], additional loss in power converters [63], and current collapse[64]. Several approaches have been reported to address these problems, including: inserting a gate dielectric to form metal-insulator-semiconductor HEMTs [65], [66], O₂ [67] and CF₄ [68] plasma treatment underneath the gate and post-metal-annealing in forming gas [69]. These methods are able to reduce the gate leakage current thus improving the ON/OFF current ratio up to 10⁸–10¹². The sources of high leakage current have been reported to be traps situated at the interface, surface and bulk [64], [70], [71], [72]. However, the origins of these traps are still under debate. Higashiwaki et al. reported that the high-temperature alloyed ohmic process generates surface traps[73]. More recently, we compare InAl(Ga)N HEMT with regrown contact and alloyed contact, it is found that HEMT device with regrown contact shows near dispersion free operation even without any passivation[48]. When the device is subject to high temperature

annealing, there is significantly current collapse as shown in Fig. 3.1, which is closely linked to the surface trap [48]. TEM images in Fig. 3.2 reveal that alloyed device has formed a surface oxide[48], while non-alloyed device shows no oxide at the surface (Fig. 3.1). But a comprehensive comparison on its effect on device leakage and dispersion is still missing. On the other hand, SiN_x and AlN passivation on GaN HEMTs have also been widely reported to effectively minimize current collapse (dynamic R_{on}) but often at the expense of an increase in leakage [46], [74].

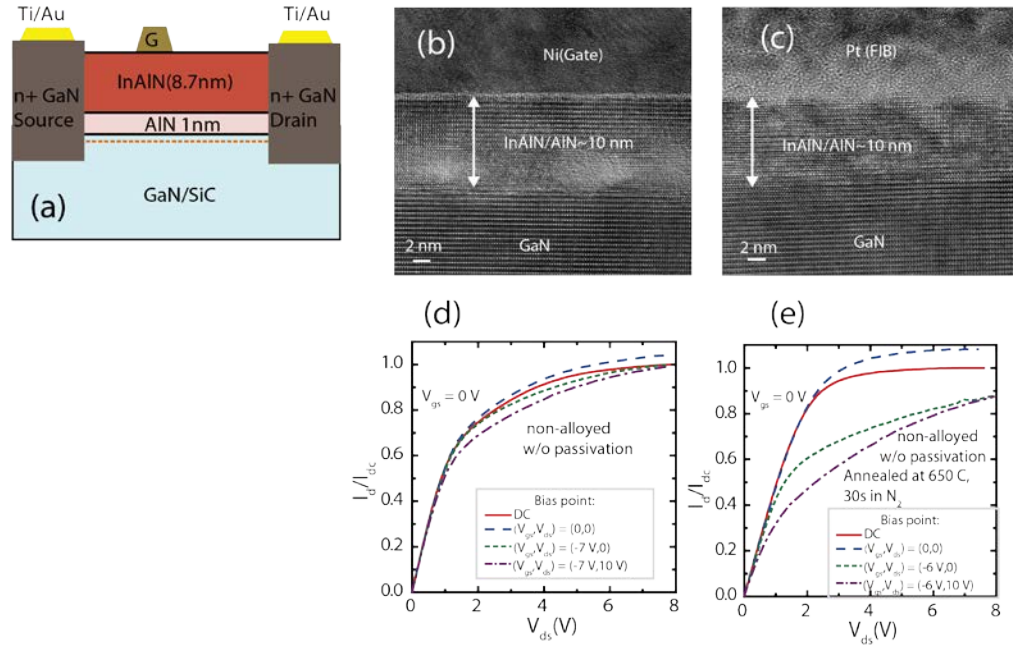


Figure 3.1 InAlN-based HEMTs with non-alloyed regrown contacts. (a) Device schematics and process flow. (b-c) Cross section HRTEM images of the gated and access regions. The entire InAlN barrier was found to be crystalline and no discernable oxides were detected by EDX (not shown). The apparent contrast within the InAlN barrier resulted from the TEM sample preparation damage. (d) Pulsed I-Vs using 300 ns pulses and a duty cycle of 0.5 ms, showing nearly dispersion free operation without any passivation. (e) Large dispersion is observed when subjecting the as-processed devices with no passivation to a high temperature annealing, indicating formation of undesired surface states leading to a large virtual gate [48].

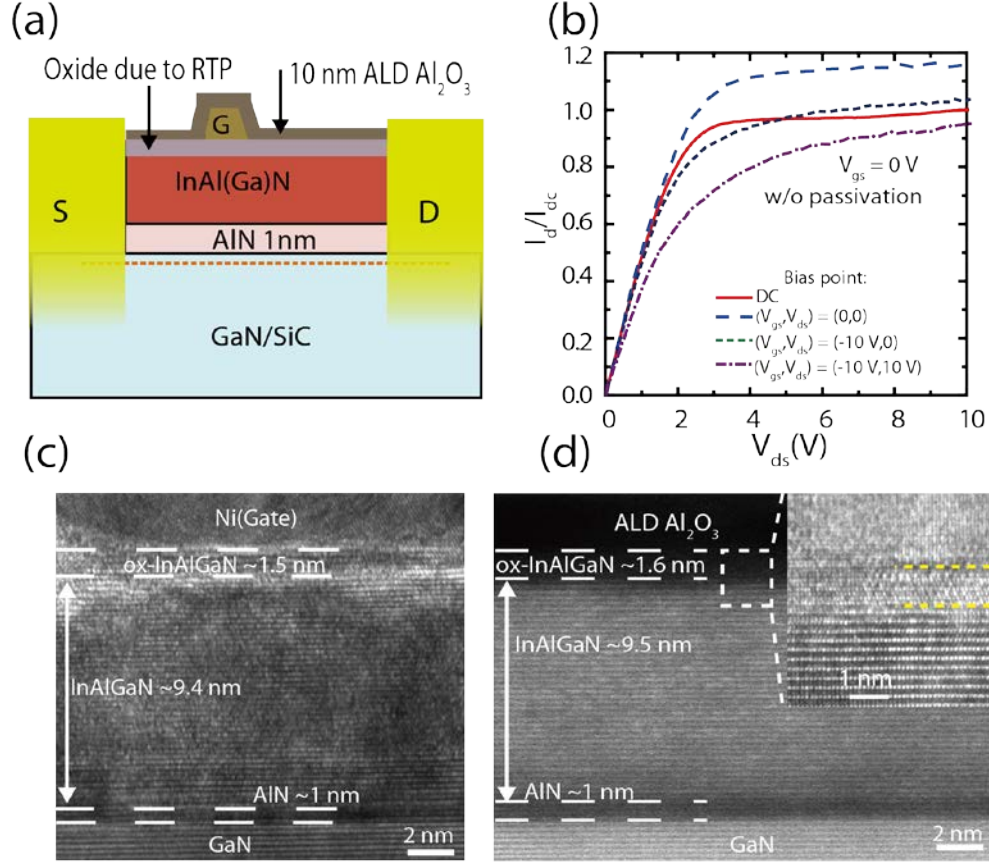


Figure 3.2 InAlN-based HEMTs with alloyed ohmic contacts. (a) Device schematics and process flow. (b) $I_d - V_{ds}$ curves of as-processed HEMTs without passivation, showing a large DC-RF dispersion. (c-d) STEM and HRTEM images showing the presence of a thin oxygen-rich layer on the surface of InAlGaN HEMTs under the gate and access region, formed during the ohmic annealing process. The inset shows this oxide layer is largely crystalline [48].

In this chapter, we report on ultralow-leakage GaN HEMTs on Si without employing any gate dielectrics, which employed non-alloyed regrown ohmic contacts, then we compare them to HEMT devices with alloyed ohmics. By avoiding the high-temperature alloying process, HEMTs with non-alloyed ohmic contacts show a high ON/OFF current ratio $>10^{11}$ and a record low leakage $\sim 10^{-12}$ A/mm, about 10^6 lower than devices with alloyed contacts. A lower subthreshold slope and a higher

breakdown voltage have also been observed. Consistent with the observation in InAlN HEMTs, AlGa_N HEMTs with non-alloyed regrown ohmic contacts also show smaller current dispersion compared to the HEMT devices with alloyed ohmics.

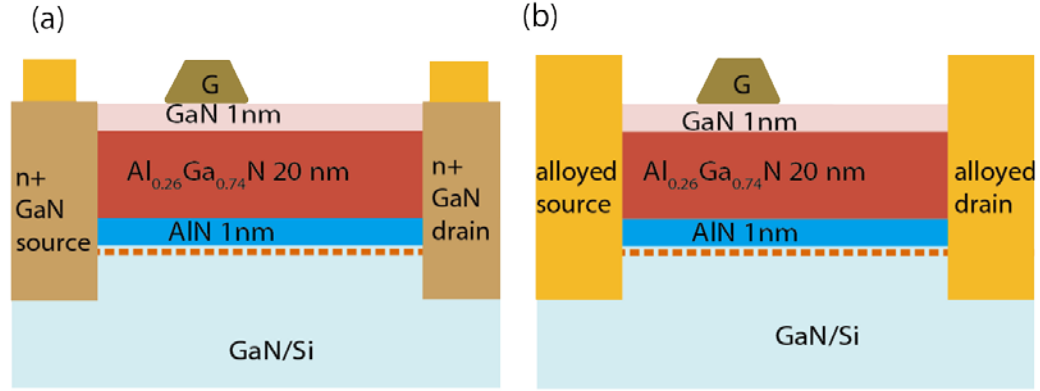


Figure 3.3 Schematic cross section of AlGa_N/Ga_N HEMT on Si with (a) non-alloyed contacts regrown by MBE and (b) alloyed contacts[71].

3.2 Experiments

Schematic cross-sections of HEMT devices with non-alloyed and alloyed ohmic contacts are shown in Fig. 3.3(a) and Fig. 3.3(b), respectively. The HEMT structure consists of a 1 nm GaN cap, 20 nm Al_{0.26}Ga_{0.74}N barrier, 1 nm AlN spacer and a GaN channel on 1.3 μm semi-insulating GaN buffer grown by metal organic chemical vapor deposition (MOCVD) on 6" Si substrates. The smooth surface has been confirmed by atomic force microscopy (AFM) as shown in Fig. 3.4 showing a RMS value of 0.63 nm for a 10 μm \times 10 μm area scan.

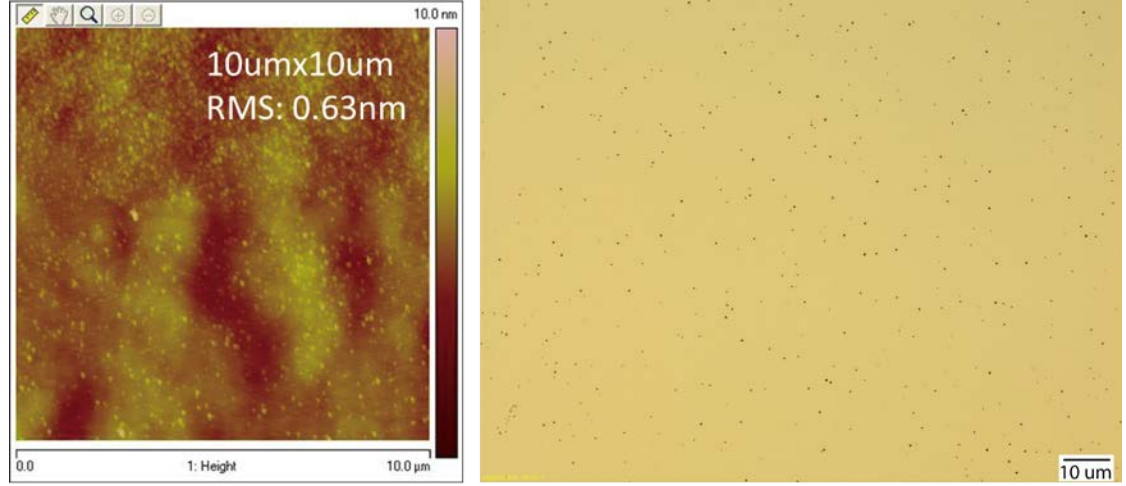


Figure 3.4 (a) AFM image of an epitaxial layer on AlGaN HEMT on Si substrate with an area of $10\ \mu\text{m} \times 10\ \mu\text{m}$ and (b) optical image (Courtesy of Xiaodong Yan).

For the non-alloyed contacts, an n^+ GaN regrowth process was employed using molecular beam epitaxy (MBE) to ensure contact with the 2D electron gas (2DEG) channel, which we have routinely employed for our GaN HEMT processes for high-speed transistors, p-channel transistors, AlN/GaN/AlN quantum well transistors as well as studying ohmic contact science [13], [51],[75],[60],[76],[7],[77],[58],[78],[79]. A 200 nm thick SiO_2 mask was deposited on the sample using plasma-enhanced chemical vapor deposition (PECVD) and then patterned by reactive ion etching (RIE). The regrowth regions were etched to a depth of 40 nm using a low-damage BCl_3/Cl_2 inductively coupled plasma RIE (ICP-RIE) recipe. MBE regrowth of an 80 nm thick Si-doped ($\sim 10^{20}\ \text{cm}^{-3}$) GaN layer was performed at 660 °C. Lift-off by buffered HF removed the polycrystalline GaN that was grown on SiO_2 . It is worth noting that the device surface was protected by SiO_2 during the regrowth process, where the temperature is also much lower than that of the contact alloying process (870 °C).

Ohmic contacts to the regrowth region were formed by E-beam evaporation of 20/100 nm Ti/Au, resulting a contact resistance R_C of 0.1 $\Omega\cdot\text{mm}$. For the alloyed contact devices, a 20/100/40/50 nm of Ti/Al/Ni/Au stack annealed in N₂ ambient at 870 °C for 20 s was used, resulting in a R_C of 0.3 $\Omega\cdot\text{mm}$. Hall measurements on the non-alloyed (alloyed) devices revealed a 2DEG concentration of 7.63×10^{12} ($4.57 \times 10^{12} \text{ cm}^{-2}$) and mobility of 1620 (1420) cm^2/Vs at room temperature. A $2 \mu\text{m} \times 50 \mu\text{m}$ ($L_g \times W_g$) gate was defined by optical photolithography, followed by a 40/100 nm Ni/Au gate metallization. The gate-to-drain spacing (L_{gd}) and the gate-to-source spacing (L_{gs}) are 4.75 and 2 μm , respectively. There was no passivation applied for any of the devices.

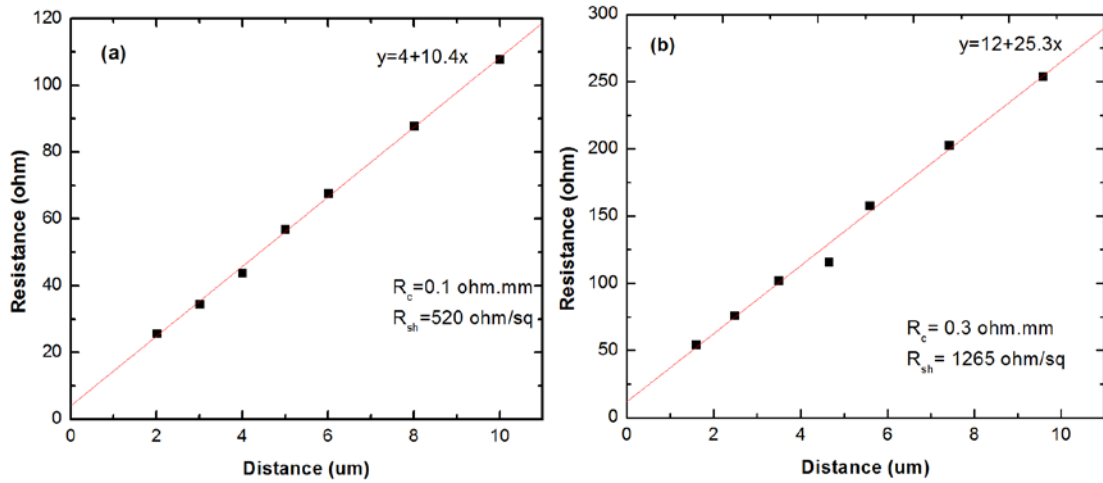


Figure 3.5 TLM results of AlGaIn/GaN HEMT on Si with (a) non-alloyed contacts regrown by MBE and (b) alloyed contacts, showing contact resistance of 0.1 and 0.3 ohm.mm, respectively.

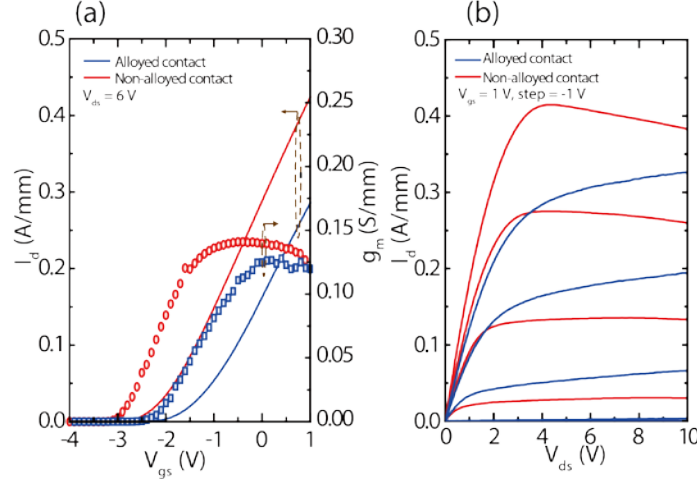


Figure 3.6 (a) Linear-scale transfer curves at $V_{ds} = 6$ V by sweeping V_{gs} from 1 to -4 V and (b) common-source I - V characteristics, of the HEMTs[71].

3.3 Results and Discussion

The linear-scale transfer curves and DC common source characteristics are shown in Fig. 3.6. The non-alloyed (alloyed) HEMTs show an output drain current density 0.42(0.29) A/mm at $V_{gs} = 1$ V and $V_{ds} = 6$ V and a peak extrinsic transconductance g_m 142(126) mS/mm, which is expected since the non-alloyed device has a lower contact resistance and sheet resistance. The threshold voltage extracted from linear extrapolation of the transfer curve at peak g_m (Fig. 3.6 (a)) is -2(-1.4) V for non-alloyed (alloyed) HEMTs. Transmission electron microscopy imaging shown in Fig. 3.7 revealed that under the gate metal no additional insulator formed in the non-alloyed device, which is different from Refs.[6],[67]. The apparent drain conductance of the alloyed device is observed to be large under the measurement conditions used, which is attributed to the severe trapping effects (also see Fig. 3.9) and worthy of a separate study to gain a full understanding. Fig. 3.8(a) shows the

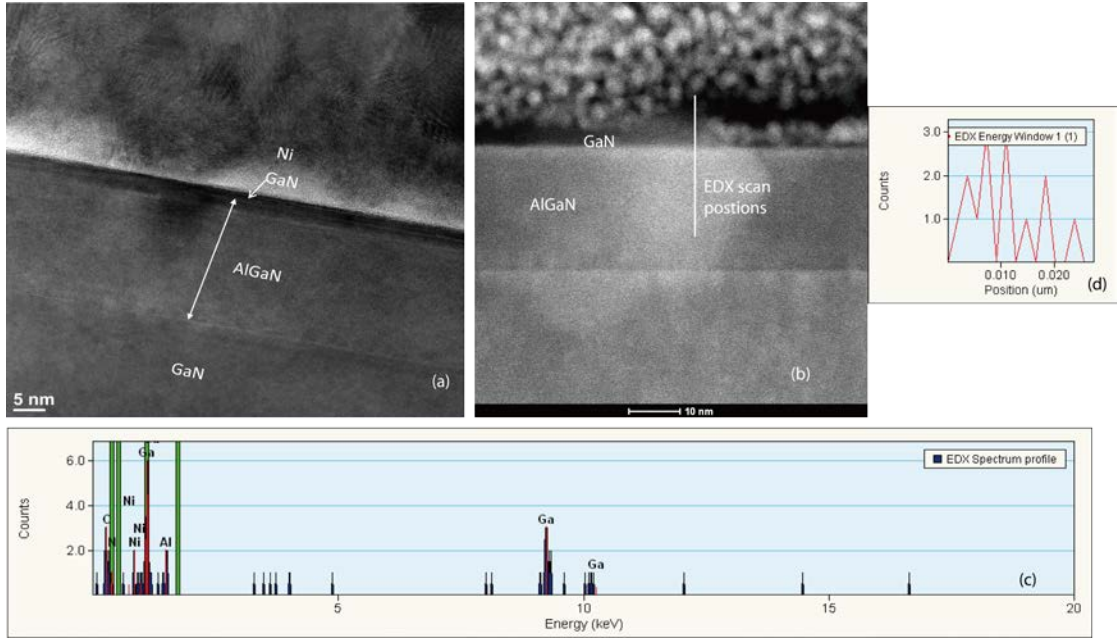


Figure 3.7 (a) Cross section HRTEM image of the gated region of an AlGaIn HEMT on Si with non-alloyed contacts. The entire AlGaIn barrier and GaN cap was found to be crystalline and no discernable oxides were detected by EDX scan along the GaN/AlGaIn layers as shown in (b) and (c) the EDX spectrum. As seen from the profile of O counts along scan direction in (d), the O signal is very small and no peak at the GaN surface. The apparent contrast within the AlGaIn barrier resulted from the TEM sample preparation damage.

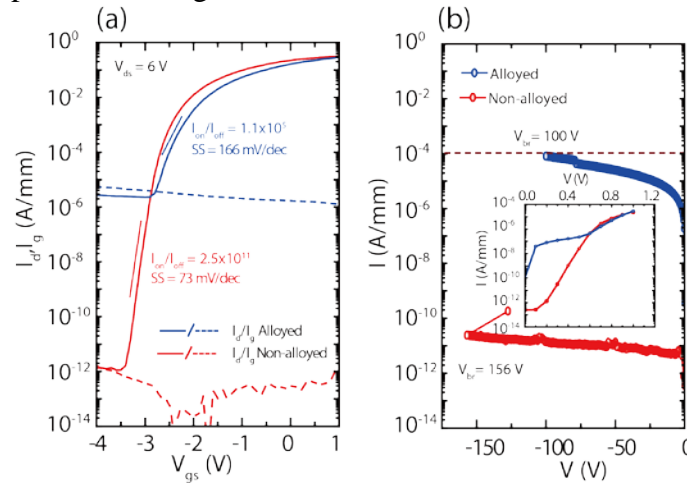


Figure 3.8 (a) Semi-log-scale transfer curves at $V_{ds} = 6$ V and (b) gate stack diode I - V curves showing breakdown voltages, of alloyed and non-alloyed device[71].

semi-log-scale transfer curves for both HEMTs measured at $V_{ds} = 6$ V. The gate leakage current reduces from $\sim 10^{-6}$ to $\sim 10^{-12}$ A/mm at off state, which is close to the record-low leakage current in GaN HEMTs on any substrate [69]. Moreover, the

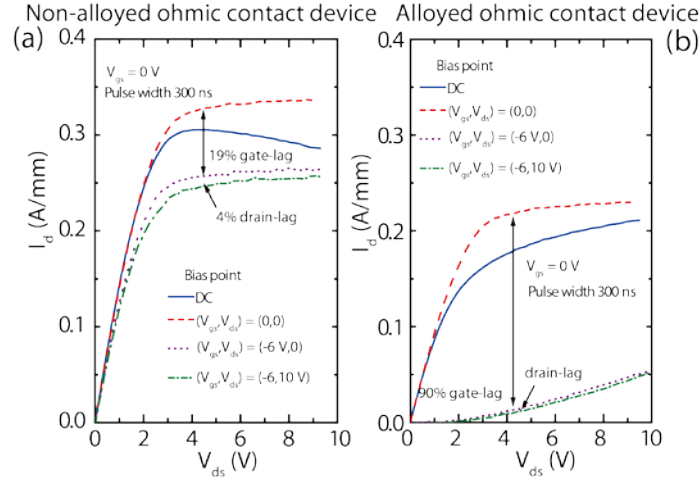


Figure 3.9 Pulsed I - V measurements in air at $V_{gs} = 0$ V, with a 300 ns pulse width and 0.5 ms period for the (a) non-alloyed and (b) alloyed devices[71].

subthreshold slope (SS) decreases from 166 to 73 mV/dec, approaching the theoretical limit at 300 K. The gate diode I - V characteristics are shown in Fig. 3.8(b). The alloyed HEMT shows a soft breakdown, approaching 100 V at 100 μ A/mm (Fig 3. 8(b)). The current in the non-alloyed HEMT stays low ($<10^{-10}$ A/mm) till 156 V where the current increases sharply due to field crowding near the gate edge since neither of the devices employed field plates. From the forward characteristics (shown in the inset of Fig. 3. 8 (b)), an apparent Schottky barrier height of 1.25(0.81) eV and an ideality factor of 1.1(4.2) are extracted for the non-alloy (alloyed) devices. An ideality factor close to unity in the non-alloyed devices indicates the Schottky barrier height should be at least 1.25 eV between Ni and pristine (Al)GaN surface. The lower extracted barrier height along with a high ideality factor is a signature of high gate leakage.

Pulsed I - V measurements are commonly employed to probe electron trapping/emission; minimal current collapse corresponds to either no trapping/emission or extremely fast trapping/emission. The results performed in air are shown in Fig. 3.9, using a 300 ns pulse width and a 0.5 ms pulse period with the following quiescent bias points (V_{gs} , V_{ds}): (0 V, 0 V) as the cold pulse, (-6 V, 0 V) for gate lag, and (-6 V, 10 V) for drain lag. Gate lag reduces from 90% in the alloyed device to 19% in the non-alloyed device. The finite gate lag in the non-alloyed devices could stem from local air breakdown, residue traps, etc. Drain lag for the non-alloyed HEMTs was observed to be 4% while the lag in the alloyed HEMTs couldn't be determined due to its severe gate lag. The small current collapse in the non-alloyed devices correlates well with its low gate leakage: the low leakage prevents electrons being trapped within hundreds of microseconds when the device is held at the off state. On the other hand, the high leakage in the alloyed device facilitates electron trapping and the electron emission rates from the traps are too low to recover the current, thus a severe current collapse.

It is also interesting to compare the DC and cold pulse curves. Both devices exhibit well-behaved cold pulse I_d - V_{ds} curves: a linear increase in current followed by saturation with a negligible output conductance owing to the large L_g . In the non-alloyed devices, the apparent output conductance is negative, attributable to self-heating. However, in the alloyed devices, a positive output conductance is seen, consistent with the hypothesis that a large number of traps exist and communicate with the gate/channel within the time frame investigated in this work. Traps have complex distributions spatially as well as in the energy space, thus exhibiting complex dynamic

behavior under different excitations (bias, temperature, photons). Understanding electron emission /trapping mechanisms merits another study.

The high temperature ohmic annealing process in AlGa_N HEMTs (typically > 800 °C) has been reported to be responsible for surface Fermi level pinning near mid-gap through traps arising from oxygen incorporation [73][48]. Such traps can contribute to a high gate leakage by trap-assisted tunneling, hopping conduction [72] and surface barrier thinning [64],[80]. In our process, increase in oxygen at the HEMT surface was indeed confirmed by x-ray photoelectron spectroscopy (XPS) and a subsequent high-temperature annealing on unpassivated devices with non-alloyed contacts degraded the device performance in terms of dispersion and device speed [48]. HEMTs with non-alloyed contacts avoid unfavorable high temperature processes, thus effectively suppressing the leakage commonly observed in AlGa_N HEMTs. Alternatively, a suitable capping material can be used during the contact alloying process to protect the HEMT surface. This work also suggests that the as-grown AlGa_N barrier is reasonably insulating with favorably low trap densities. For real world applications, a moisture barrier/passivation layer is typically employed and such processes need to be carefully investigated similar to that of high-quality gate dielectrics. Extreme care needs to be taken during subsequent device process steps to minimize introduction of damage.

3.4 Conclusion

In this section, we report on AlGa_N/Ga_N HEMTs on Si with non-alloyed regrown ohmic contacts showing a record-low leakage current, about six orders of magnitude smaller than that of the conventional devices with alloyed ohmics.

CHAPTER 4

GAN POLARIZATION-DOPED POWER DEVICES

4.1 Advantages of GaN Polarization-doped Power Devices

With a wide bandgap, a high breakdown electric field and a high saturation drift velocity, GaN based devices have demonstrated great potentials for high-frequency, high-power applications[6], [26], [29], [61], [81]. More recently, larger bandgap semiconductors such as Ga_2O_3 and AlN based power devices are emerging for the future power switching applications owing to their high Baliga's figure-of-merit (FOM) [24], [25]. However, for the wide bandgap semiconductors, the high activation energy of p-type dopant is a common issue; e.g. 170 meV for Mg in GaN and p-type Ga_2O_3 is yet to be demonstrated. There is another big "hidden problem": all deep dopants suffer from frequency dispersion. Given an activation energy of Mg in GaN being $\sim 6 k_B T$, at room temperature, roughly about 1-10 % of Mg acceptors are ionized in charge neutral GaN:Mg. But, in the depletion region of a p-n junction, all Mg acceptors are ionized since the Fermi level is way above the valence band edge (i.e. states below the Fermi levels are occupied by electrons). For a typical doping concentration of 10^{18} - 10^{19} cm^{-3} , the large ionized Mg acceptor concentration sets a small depletion width on the p-side at DC or low frequencies, which is extremely valuable since it results in a high punch-through voltage, i.e. a very high voltage is needed to ionize all the Mg acceptors thus depleting all the holes. However, under

high frequencies, thermal ionization of the acceptors is too slow to follow the fast changing voltage; as a result, the fast responding holes determine the electrostatics of

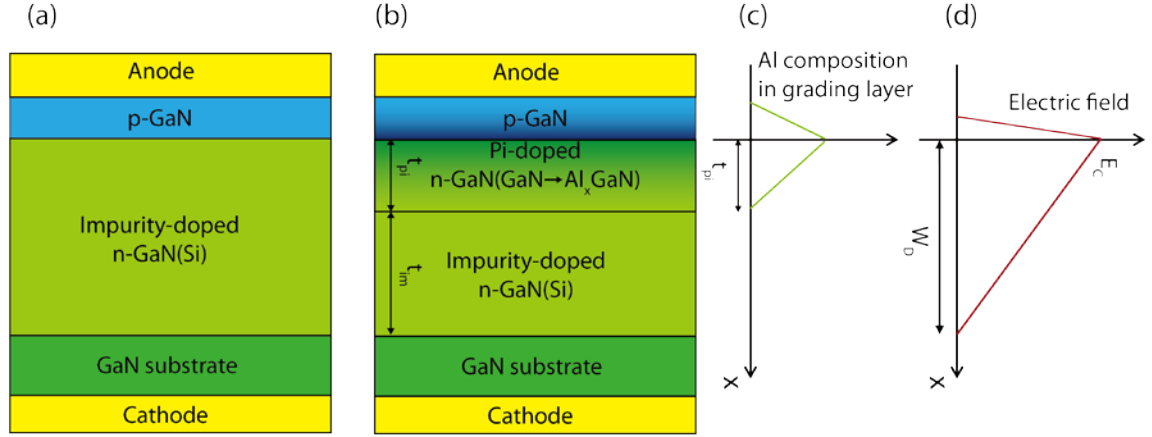


Figure 4.1 (a) Impurity-doped (*Imp-doped*) and (b) polarization-doped (*Pi-doped*) GaN high-voltage p-n junction diodes with a uniformly doped drift region. (c) Al composition in the graded layers in the *Pi-doped* device and (d) the corresponding electric field distribution under the breakdown voltage condition.

the device. This implies that the device punch-through voltage is determined by the acceptor concentration at DC and low frequencies but determined by the hole concentration at high frequencies. This frequency dispersion effect was first measured and evaluated by Kozodoy et al [82]. The small signal capacitance of GaN p-n junctions was observed to drop at a frequency as low as 60 kHz due to the widening of the depletion region[82].

To overcome the large activation energy barrier to obtain holes and the associated frequency dispersion problem, polarization-induced doping by compositionally grading $\text{Al}_x\text{In}_y\text{Ga}_{1-x-y}\text{N}$ has been demonstrated to achieve both n- and p- type doping, thanks to the spontaneous and piezoelectric polarization effects in the GaN material

system [33], [34]. Furthermore, in power devices, it is desirable to place a wider bandgap material (e.g. AlGaN over GaN) at the highest field region of the device.

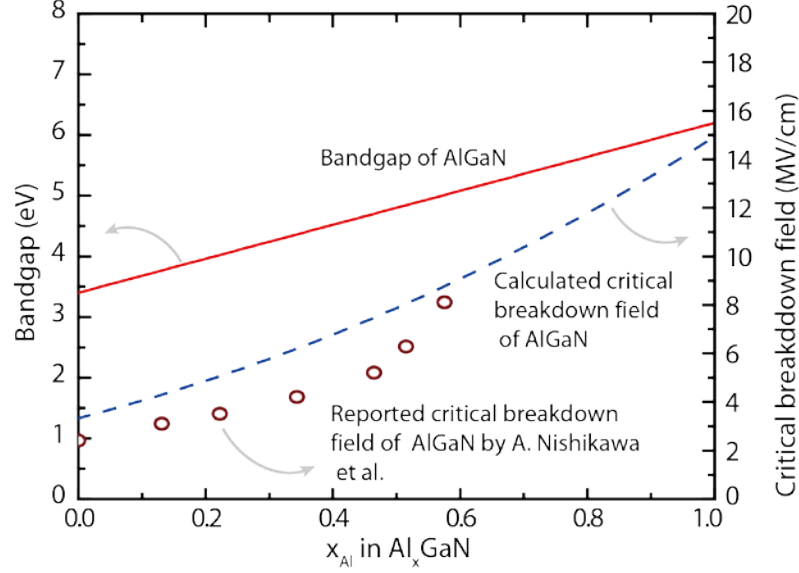


Figure 4.2 Bandgap and critical breakdown field of $\text{Al}_x\text{Ga}_{1-x}\text{N}$ as a function of x_{Al}

In this section, the Baliga's FOMs of GaN *Pi-doped* and impurity-doped (*Imp-doped*) high voltage unipolar devices are compared using analytical models. In both types of devices the net doping concentration in the drift region is kept to be uniform. It is found that $R_{on,sp}$ in *Pi-doped* devices is about 1/3- 2/3 of that in the *Imp-doped* devices for the same breakdown voltage at the non-punch-through case.

The devices chosen in this study are conventional *Imp-doped* and *Pi-doped* GaN p-n junction diodes as shown in Fig. 4.1 (a) and (b), since a p-n diode is an essential building block for high voltage devices like VDMOS, IGBT etc. The *Imp-doped* diode has an impurity doped (typically $\text{Si} < 1 \times 10^{17} \text{ cm}^{-3}$) n-type drift region on GaN substrate and an impurity doped p-type GaN (typically $\text{Mg} > 1 \times 10^{18} \text{ cm}^{-3}$). For the *Pi-doped* diode, the drift region consists of two parts: impurity doped GaN and the *Pi-*

doped layer by linearly grading GaN to Al_{x0}GaN on Ga-polar GaN substrate for achieving n-doping. The top p-type layer can be obtained by linearly grading Al_{x0}GaN back to GaN.

For the unipolar FOM, an abrupt junction and an ideal parallel-plane condition can be assumed while neglecting the junction curvature effect. The electric field profile at the device breakdown voltage (BV) is shown in Fig. 4. 1(d), where the peak electric field reaches the critical breakdown field E_c and the depletion depth reaches the total drift region W_D . The smooth electrical field in the *Pi-doped* device is imposed by the same doping concentration in the *Pi-doped* region as the *Imp-doped* GaN underneath. For *Imp-doped/Pi-doped* GaN device, total drift region and the doping are expressed as

$$W_{D_Imp} = \frac{2BV}{E_{c_GaN}}, N_{D_Imp} = \frac{\epsilon_s E_{c_GaN}^2}{2qBV}, \quad (4.1)$$

$$W_{D_Pi} = \frac{2BV}{E_{c_AlGaN}(x0_{Al})}, N_{D_Pi} = \frac{\epsilon_s E_{c_AlGaN}^2(x0_{Al})}{2qBV} \quad (4.2)$$

where the total drift region and doping concentration is a function of critical breakdown field of Al_{x0}GaN (E_{c_AlGaN}) instead of GaN (E_{c_GaN}) for *Pi-doped* devices. The difference in permittivity between AlGaN and GaN is neglected. The thicknesses of the *Pi-doped* region t_{Pi} and the *Imp-doped* region t_{Imp} in the *Pi-doped* device can be calculated to be

$$t_{Pi} = \frac{\sigma_\pi(x0_{Al})}{N_{D_Pi}}, t_{Imp} = W_{D_Pi} - t_{Pi} \quad (4.3)$$

where $\sigma_\pi(x0_{Al})$ is the net polarization charge due to the difference in the spontaneous and piezoelectric polarization between Al_{x0}GaN and GaN. The ideal specific on-

resistance $R_{on,sp}$ considering only the unipolar electron conducting in the drift region for *Imp-doped/Pi-doped* GaN device are

$$R_{on,sp_Imp} = \frac{W_{D_Imp}}{q\mu_n N_{D_Imp}} = \frac{4BV^2}{\epsilon_s \mu_n E_{c_GaN}^3}, \quad (4.4)$$

$$R_{on,sp_Pi} = \frac{t_{Imp}}{q\mu_n N_{D_Pi}} + \int_0^{t_{Pi}} \frac{dz}{q\mu_n(x_{Al}) N_{D_Pi}}$$

$$= \frac{4BV^2(\epsilon_s E_{c_AlGaN}(x0_{Al}) - q\sigma_\pi(x0_{Al}))}{\epsilon_s^2 \mu_n E_{c_AlGaN}^4(x0_{Al})} + \int_0^{t_{Pi}} \frac{2BVdz}{\epsilon_s \mu_n(x_{Al}) E_{c_AlGaN}^2(x0_{Al})} \quad (4.5)$$

where ϵ_s and μ_n is the permittivity and electron mobility of GaN, respectively. $\mu_n(x_{Al})$ is the Al-composition dependent electron mobility in the *Pi-doped* layer. From Eqn. 4.5 it is found that the R_{on,sp_pi} of *Pi-doped* devices is a function of critical breakdown field of $Al_{x0}GaN$, polarization charge and electron mobility in the impurity and *Pi-doped* layers. All these are closely related to the final Al composition $x0_{Al}$ in the graded layer. The critical breakdown field of Al_xGaN is expected to increase with higher x_{Al} composition due to the increasing bandgap. Hudgins et al. proposed an empirical relation of E_c in direct bandgap (E_g) materials: $E_c \sim (E_g)^{2.5}$ [83]. More recently, Nishikawa et al. have experimentally demonstrated that BV increases with increasing x_{Al} in vertical p-i-n Al_xGaN diodes grown on conducting SiC substrates and reached a similar conclusion that E_c is proportional to $E_g(AlGaN)$ to the power of 2.5[84], [85]. Ideally, this conclusion should be confirmed on bulk substrates with minimal dislocation densities. However, studies on $AlGaN$ in the literature are very limited due to unavailability of high quality $AlGaN$ [86]. In this study, the following relationships are adopted:

$$E_{c_AlGaN} = 3.4 \times 10^6 \left(\frac{E_{g_AlGaN}}{E_{g_GaN}} \right)^{2.5} \text{ V/cm} ,$$

$$E_{g_AlGaN} = 6.2 \times x_{AlN} + 3.4 \times (1 - x_{AlN}) \text{ eV} , \quad (4.6)$$

The electron mobility modeling of GaN and *Pi-doped* layer are modeled following the method in Ref. [32]. For *Imp-doped* GaN layers, acoustic and optical phonon scattering, neutral and ionized impurity scattering mechanisms are considered. For *Pi-doped* layers, alloy scattering and optical phonon scattering mechanisms are considered (ideally impurity scattering is absent). The results are shown in Figure 4.3. Since the *Pi-doped* electron mobility depends on the local Al composition, an integration is used to calculate $R_{on,sp}$ (Eqn. 4.5). For a straightforward comparison with the *Imp-doped* region, an average mobility $\bar{\mu}_n$ in the *Pi-doped* region is also calculated.

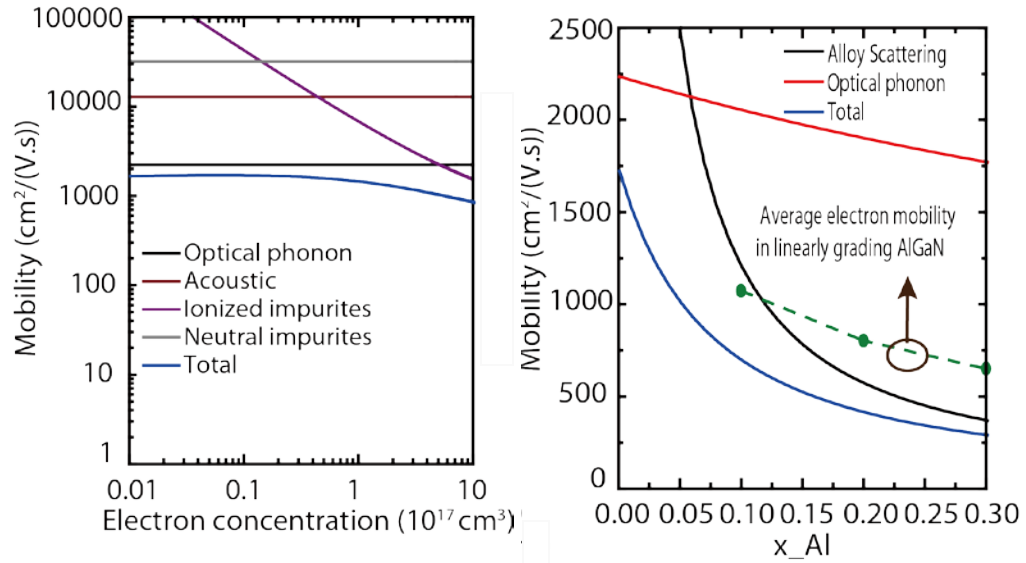


Figure 4.3 Modeled electron mobility for (a) impurity doped layer and (b) *Pi-doped* layer with different Al composition

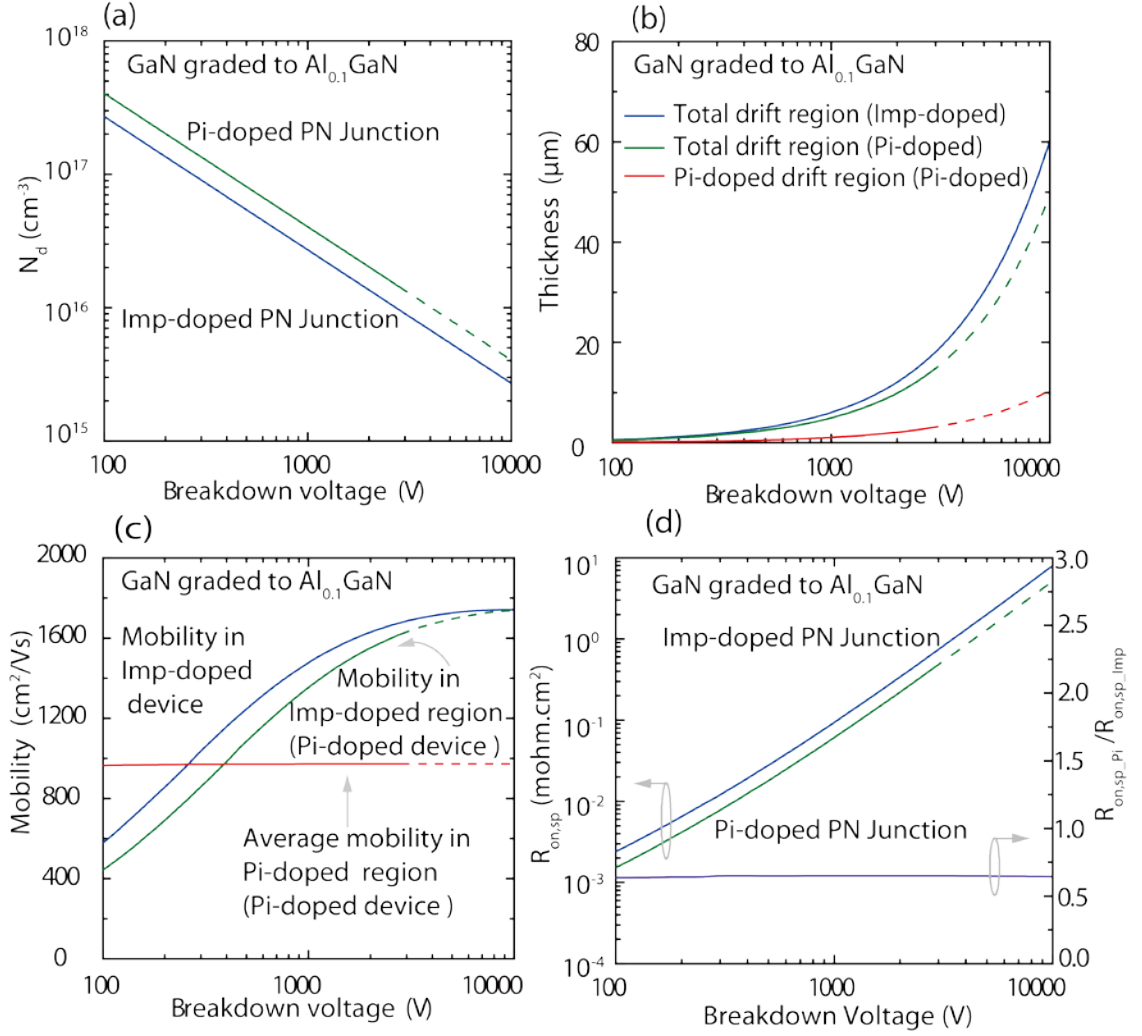


Figure 4.4 Comparison of *Imp-doped* and *Pi-doped* device by grading GaN to Al_{0.1}GaN at different BV values: (a) doping concentration, (b) total drift region and *Pi-doped* region thickness (according to Eqn. 4), (c) mobility in *Pi-doped* region and *Imp-doped* region (d) Ideal $R_{on,sp}$

It is also worth noting that by imposing the uniform doping condition in the drift region in the *Pi-doped* devices, the electric field at the interface between the *Pi-doped* layer and the *Imp-doped* layer underneath is always lower than E_{c_GaN} under the breakdown condition for $x_{0Al} \leq 0.39$:

$$E_{Interface} = E_{c_AlGaIn} - \frac{qN_{D_Pi}t_{Imp}}{\epsilon_s} = \frac{q\sigma_\pi(x_{0Al})}{\epsilon_s} \leq E_{c_GaN} \quad (4.7)$$

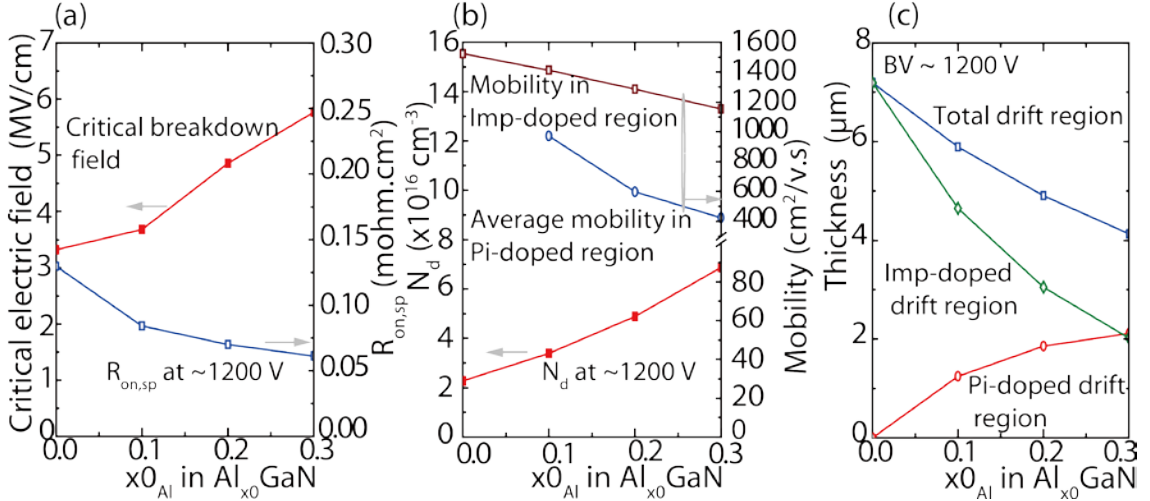


Figure 4.5 Comparison of *Imp-doped* and *Pi-doped* devices by linearly grading GaN to $Al_{x0}Ga_{1-x0}N$ where $x_{Al}=0.1 \sim 0.3$ for a target BV of ~ 1200 V: (a) Critical breakdown field and $R_{on,sp}$, (b) doping and mobility in the *Imp-doped* and *Pi-doped* region, (c) total drift region thickness, *Imp-doped* and *Pi-doped* region thicknesses.

Fig. 4.4 shows results of *Imp-doped* and *Pi-doped* devices with the *Pi-doped* layer grading from GaN to $Al_{0.1}Ga_{0.9}N$ (i.e. $x_{Al} = 0.1$). The dashed lines in Fig. 4.4 correspond to thick *Pi-doped* layer thickness $> 3 \mu m$, which is found challenging to grow based on our ongoing experimental investigations. Since the peak field is located at $Al_{0.1}Ga_{0.9}N$, for the same breakdown voltage the *Pi-doped* device can afford a thinner drift region with a higher doping concentration compared to the *Imp-doped* ones. With an increasing target BV , the required doping concentration is reduced, thus the thickness of the *Pi-doped* region increases given that the total polarization charge remains the same. The mobilities for both *Imp-doped* and *Pi-doped* layers are shown in Fig. 4.4(c) at the corresponding doping concentrations for a target BV . The average mobility in the *Pi-doped* layer shows small variation as expected (dominated by alloy scattering) while that in the *Imp-doped* layer increases from 400 to 1600 cm²/(V.s) when N_D reduces from 2×10^{17} to 2×10^{15} cm⁻³. Though the mobility in the *Pi-doped*

device is overall lower than that in the *Imp-doped* device, the higher E_c ($\text{Al}_{0.1}\text{GaN}$) leads to an overall reduction in $R_{on,sp}$: the ratio of $R_{on,sp-Pi}/R_{on,sp-Imp}$ is ~ 0.6 , as shown in Fig. 4. 4(d).

For a target BV of $\sim 1200\text{V}$, Fig. 4.5 shows the comparison between the *Imp-doped* and *Pi-doped* devices with $x_{\text{Al}} = 0.1, 0.2$ and 0.3 . By increasing the Al composition x_{Al} at the highest field region from 0 to 0.3, the critical breakdown field increases from 3.4 to 5.8 MV/cm. The total drift region is therefore reduced from 7.2 to 4.1 μm , where half of the drift region is *Pi-doped* when $x_{\text{Al}} = 0.3$. The doping concentration increases from 2.3×10^{16} to $6.9 \times 10^{16} \text{ cm}^{-3}$. Finally, $R_{on,sp}$ reduces from ~ 0.13 to $0.06 \text{ m}\Omega\cdot\text{cm}^2$.

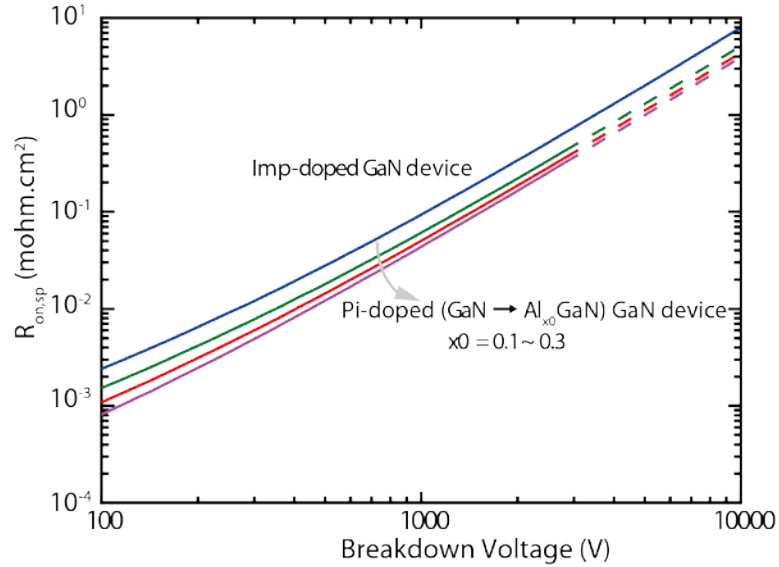


Figure 4.6 Ideal $R_{on,sp}$ versus breakdown voltage of the *Imp-doped* and *Pi-doped* GaN unipolar devices. For the *Pi-doped* GaN devices, three cases with GaN grading to $\text{Al}_{x\text{Al}}\text{GaN}$ ($x_{\text{Al}} = 0.1-0.3$) are included, where higher x_{Al} case shows lower $R_{on,sp}$

The plot of the ideal $R_{on,sp}$ versus BV is shown in Fig. 4.6. It is observed that for the same BV , $R_{on,sp}$ in the *Pi-doped* devices is about $1/3 - 2/3$ of that in the *Imp-doped* devices. This validates the performance advantage in employing *Pi-doping* for GaN

power devices. In principal, an higher reduction in $R_{on,sp}$ is expected with a higher Al composition. However, such designs are most likely limited by high quality epitaxy of thick graded layers due to lattice mismatch between AlGaN and GaN.

In conclusion, the FOM of high voltage unipolar devices with a uniform doping in the drift region is compared in GaN polarization-doped and impurity-doped devices. By linearly grading GaN to $Al_{x0}GaN$ with $Al_{x0}GaN$ situated at the highest field region of the device, the ideal $R_{on,sp}$ of the *Pi-doped* device can be $1/3 - 2/3$ of that of the *Imp-doped* device. This suggests that *Pi-doped* GaN devices show great potential for high-voltage power switching applications.

4.2 High-Voltage GaN Impurity and Pi-doped p-n Diodes

High voltage GaN p-n diodes are the fundamental segment for the development of GaN JFET, VDMOS and IGBTs. In this part, we will first discuss high-voltage GaN impurity-doped p-n diodes with high quality epitaxy and a low threading dislocation densities of $\sim 10^6 \text{ cm}^{-2}$, which were grown by our collaborators in Japan using MOCVD and subsequently fabricated by Dr. Kazuki Nomoto using the Nanofabrication Facilities at the University of Notre Dame. Careful testing and analysis provide a solid understanding of these high voltage GaN p-n diodes. These devices serve as the benchmark devices for our development of polarization-doped high-voltage GaN p-n diode in terms of epitaxy quality and device performance. We discuss the progress and results on impurity-doped and *Pi-doped* GaN p-n junction devices in collaboration with IQE, followed by discussions of related challenges and solutions. The devices presented below have been mostly fabricated by Dr. Nomoto.

4.2.1 High-Voltage GaN Impurity p-n Diodes for Benchmarking

4.2.1.1 Device Fabrication

The GaN p-n diodes shown in Fig.4.7 consist of a 10 nm p^{++} GaN (Mg: $2 \times 10^{20} \text{ cm}^{-3}$)

contact layer, a 500 nm p-GaN (Mg: $1 \times 10^{18} \text{ cm}^{-3}$) layer, a 10 μm n-GaN drift region with a target Si doping concentration of $1\text{-}2 \times 10^{16} \text{ cm}^{-3}$ and reasonably low background impurity concentrations: C $\sim 1.2 \times 10^{16} \text{ cm}^{-3}$ and O $\sim 1.7 \times 10^{16} \text{ cm}^{-3}$, and 2 μm n⁺ GaN buffer layer (Si: $2 \times 10^{18} \text{ cm}^{-3}$) on a 2-inch 400 μm thick bulk GaN substrate, all grown by metalorganic vapor phase epitaxy (OMVPE or MOCVD). These target concentrations were deduced from secondary ion mass spectrometry (SIMS) measurements on calibration wafers grown under the same growth conditions. Plain-view cathodoluminescence reveals that the threading dislocation density (TDD) in the homoepitaxial GaN epilayers is low and uniform ($\sim 10^6 \text{ cm}^{-2}$), comparable to that of the bulk GaN substrates, which is at least two orders of magnitude lower than that of heteroepitaxial GaN. After growth, a thermal annealing was performed at 700 °C to activate Mg acceptors. The p-type GaN layer has a hole concentration of $7.4 \times 10^{16} \text{ cm}^{-3}$ with a mobility of $27 \text{ cm}^2/\text{V}\cdot\text{s}$ ($R_{sh} \sim 60 \text{ k}\Omega/\text{sq}$) at 25 °C as determined by the Hall effect measurements, .

The schematic cross-sections of the fabricated GaN diodes without (w/o) and with field plate (FP) are shown in Fig. 4.7. The FP is formed by extending a metal layer over the entire mesa of the diode covered by spin-on-glass (SOG), in order to reduce reverse leakage current thus improving breakdown voltage. The fabrication process starts with a thick SiO₂ deposition by plasma-enhanced chemical vapor deposition (PECVD), followed by lithography and a buffered oxide etch (BOE) to form a hard mask with slant sidewalls. A Cl₂ based inductively coupled plasma (ICP) dry etch at an ICP power of 250 W, an RIE power of 20 W and a pressure of 5 mTorr was used to define the mesa with slant sidewalls, which are transferred from the SiO₂ hard mask.

The bottom diameter of the diode mesa ranges from 67 to 707 μm . The Pd/Ni/Pt (30/30/30 nm) circular anodes were formed on the p^{++} GaN layer, after which a SOG film of ~ 200 nm was coated and cured at 425 $^{\circ}\text{C}$ for 30 mins. The anode electrodes were not alloyed purposely but the curing process for SOG affected the metal stack slightly. The transfer length measurement (TLM) (Fig. 4.8) shows that the contact resistance on p-GaN is about $1.6 \times 10^{-4} \Omega \cdot \text{cm}^{-2}$ and the p-region sheet resistance of 63 $\text{k}\Omega/\text{sq}$, which is consistent with the hall measurement result 60 $\text{k}\Omega/\text{sq}$. Contact holes were subsequently formed by wet etch and a Ti/Al/Au stack was deposited to form the FP structure. Finally, a non-alloyed Ti/Al/Au (50/200/50 nm) electrode was formed on the rear surface of the GaN substrate.

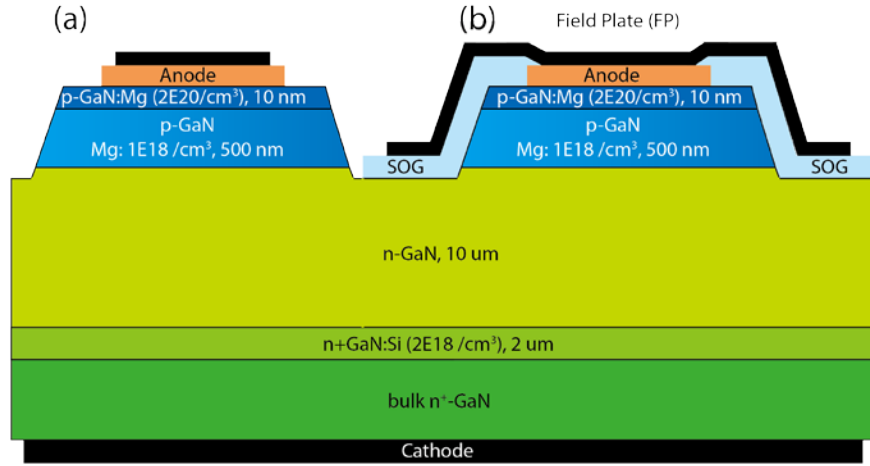


Figure 4.7 Schematic cross-sections of the GaN-on-GaN p–n junction diodes (a) without (w/o) field plate (FP) and (b) with FP. (courtesy of Dr. Kazuki Nomoto)

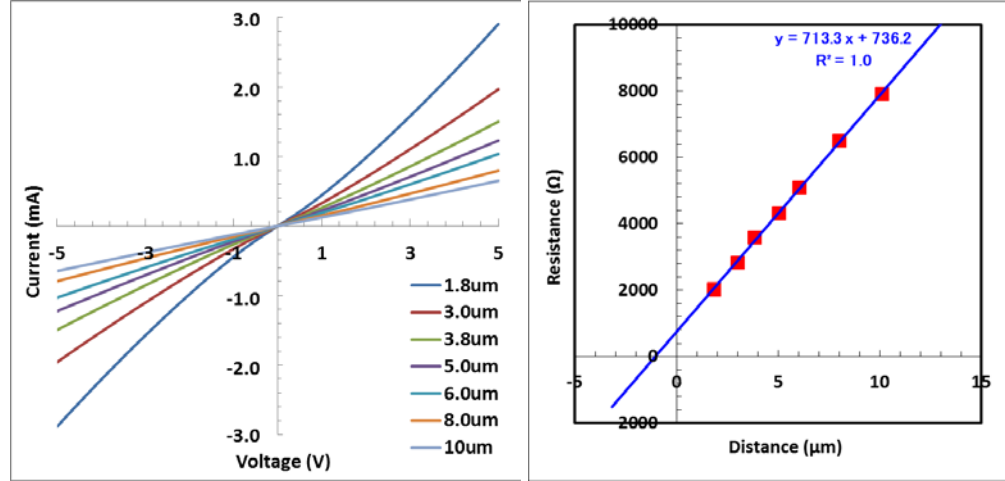


Figure 4.8 P-type region TLM I-V curves and extraction of contact resistance showing a contact resistance of $1.6 \times 10^{-4} \text{ cm}^{-2}$ and a sheet resistance of $63 \text{ k}\Omega/\text{sq.}$ (courtesy of Dr. Kazuki Nomoto)

For the device results shown in this section, at least 3 devices of each type with $BV > 500 \text{ V}$ were measured and the best device characteristics are shown since they best represent the potential of the GaN-on-GaN devices. *The bottom diameter of the mesa* is used to calculate the diode size unless otherwise noted. Substrates were not thinned.

4.2.1.2 DC Characteristics

Assuming a one-sided p+-n junction since the Mg doping concentration in p-GaN is about 100x the Si doping concentration in n-GaN, the net doping concentration ($N_D - N_A$) in the n-GaN drift layer can be extracted from capacitance–voltage ($C-V$) measurements:

$$N_D - N_A = -\frac{2}{q\epsilon_s} \frac{1}{d \left(\frac{1}{C^2} \right) / dV} \quad (4.8)$$

where N_D/N_A are donor/acceptor concentrations in n-GaN, q the electron charge and ϵ_s the permittivity of GaN. A representative plot of $1/C^2$ as a function of the reverse

voltage up to 500 V on our p-n diodes is shown in Fig. 4. 9(a) and the extracted net doping profile is shown in Fig. 4. 9 (b). In our n-GaN drift layer, $N_D - N_A$ is found to be around $1.0 \times 10^{16} \sim 1.2 \times 10^{16} \text{ cm}^{-3}$, which is comparable to the target Si concentration of $1\text{-}2 \times 10^{16} \text{ cm}^{-3}$.

Fig. 4.10 shows the representative forward I - V characteristics of the GaN p-n junction diodes with and w/o FP at room temperature, measured using a Keithley 4200 semiconductor analyzer. These GaN p-n diodes behave like a textbook p-n junction, sweeping a current range over 14 orders of magnitude. When $V_f < 2 \text{ V}$, the diode current is too low to be measured by our equipment. For $2 \text{ V} < V_f < 2.5 \text{ V}$, the diode ideality factor is nearly constant ~ 2.0 , suggesting a Shockley-Read-Hall (SRH) recombination dominated current. The ideality factor steadily drops to ~ 1.3 near 2.8 V, signifying the ideal diode diffusion current overwhelms the SRH current in this bias window. The upturn of the ideality factor beyond 2.8 V is due to the effects of the diode series resistance. A careful analysis of temperature dependent I - V s shows a

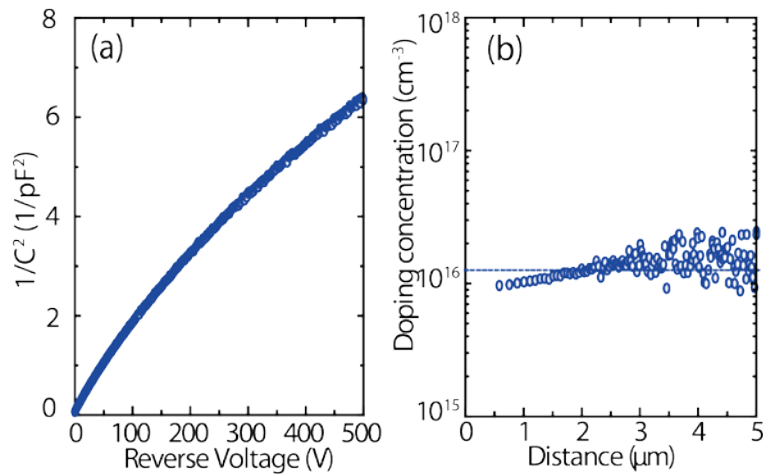


Figure 4.9 (a) Measured $1/C^2$ versus reverse voltage up to 500 V in the GaN p-n diodes and (b) extracted carrier density profile in the n-GaN drift layer [81].

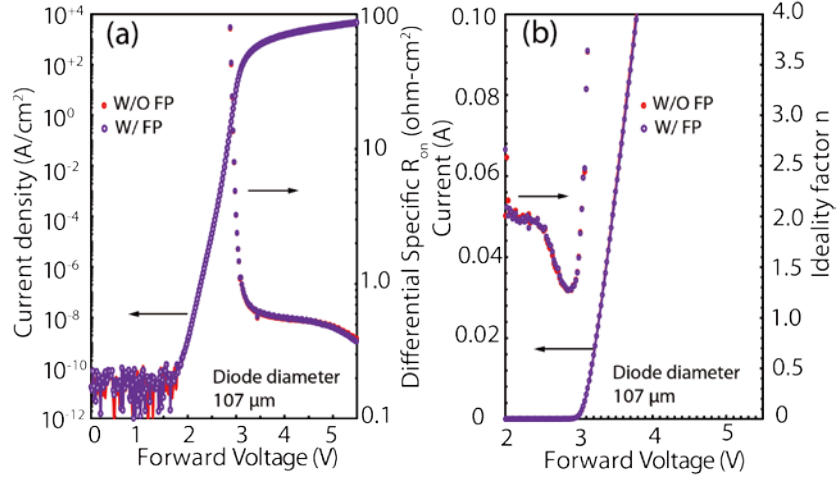


Figure 4.10 Forward I - V characteristics of GaN p-n junction diodes w/ and w/o FP (a) in logarithm scale and R_{on} w/o considering lateral current spreading, and (b) in linear scale and the ideal factor of the diodes [81].

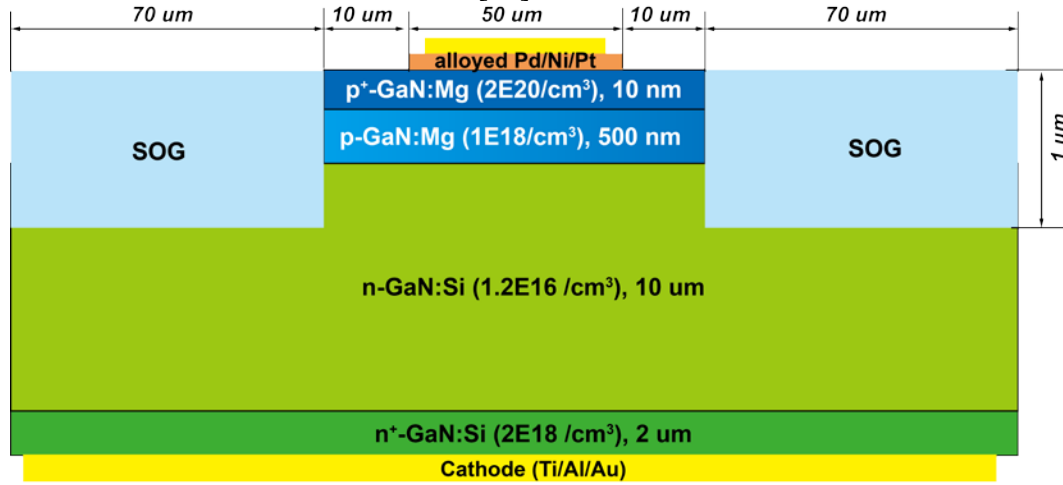


Figure 4.11 Schematic cross-section of the GaN-on-GaN p-n junction diodes used in the TCAD simulation.

SRH lifetime of ~ 12 ns in our GaN p-n diodes [87]. The apparent turn-on voltage of the diodes is about 3.0 V, expected based on the GaN bandgap.

Using the mesa bottom-diameter of 107 μm , a differential specific on-resistance ($R_{on}=dV/dI$) of ~ 0.4 $\text{m}\Omega\cdot\text{cm}^2$ can be obtained at a current density ~ 3 kA/cm^2 . To more accurately calculate the differential specific on-resistance, the current spreading

effect for the vertical devices should be considered. We have employed two approaches to investigate this problem: TCAD simulation and space-resolved electroluminescence measurement.

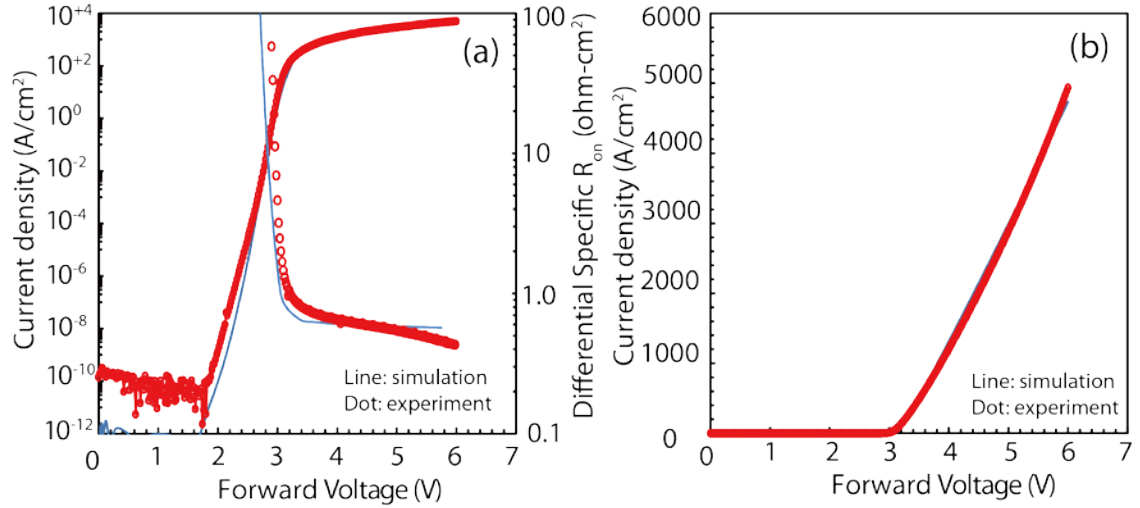


Figure 4.12 Comparison of simulated and measured GaN p-n junction diodes I-V characteristics in (a) logarithm scale and (b) linear scale.

For TCAD simulation, a bottom mesa diameter of 70 μm with a metal anode diameter of 50 μm GaN p-n Diode has been used as shown in Fig. 4.11. The model considers both drift-diffusion and recombination currents. The mobilities for electrons and holes μ_n/μ_p were set to be 1000/20 $\text{cm}^2/(\text{V}\cdot\text{s})$, respectively. The electron and hole lifetime used for recombination current was $\tau_n/\tau_p = 1/1$ ns. Additional anode and cathode resistances R_a/R_c of 320/60 ohm were added in the simulation, which corresponds to 0.16 $\text{mohm}\cdot\text{cm}^2$ and 0.03 $\text{mohm}\cdot\text{cm}^2$ at the anode and the cathode, respectively. The simulated results for the p-n junction are compared to the measured p-n junction results in both logarithm scale and linear scale in Fig. 4.12. From Fig. 4.12(a), we can see there is a reasonable good fit of the I-V as well as the differential

on-resistance. The off-state leakage of the measured p-n diode is limited by the measurement resolution of our test system. In Fig. 4.12(b), we see a very good fit in the linear scale I-V fitting. This validates the physical model employed in our simulation and calibration of the values of various parameters in the model. The current density profile at $V_{ds} = 6$ V is shown in Fig. 4.13(a), and the current profile along x direction at the y-cut along the middle of the drift region is shown in Fig. 4.13 (b). As we can see, the current density under the mesa region J_0 is quite uniform, while the current density outside the mesa region starts to decreases.

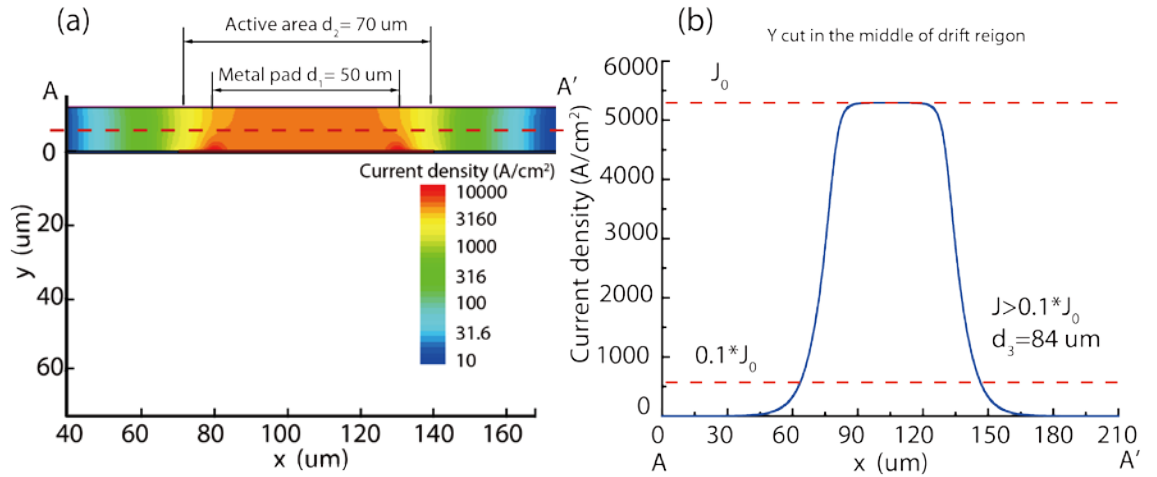


Figure 4.13 (a) Map of simulated current density of the GaN p-n diode with a drift layer $L_d = 10$ μm where a high current density of 4732 A/cm^2 (normalized to the diode mesa width) is reached at 6 V. (b) Current density profile across the middle of the drift region.

We define the effective current carrying width of the diode by the two points where the current density drops to $10\%J_0$, where J_0 is the maximum current density in the middle of the diode. At a nominal current density of 4732 A/cm^2 (normalized to the diode mesa width d_2), we can get an effective diode width d_3 of 84 μm . Considering

the diode mesa width being 70 μm , a current spreading length of 7 μm at each side can be calculated.

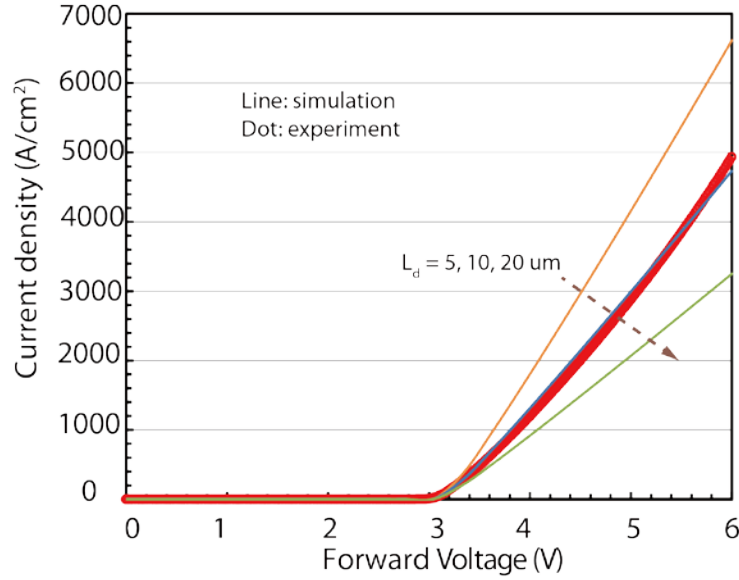


Figure 4.14 Simulated I-V characteristics of GaN p-n junction diodes with different drift region thicknesses: $L_d=5, 10, 20 \mu\text{m}$. The dot line is for experimental data with $L_d = 10 \mu\text{m}$.

We also varied the drift region thickness from 5 to 20 μm and the simulation results are shown in Fig. 4.14. With a thicker drift region thickness, the current density at a fixed forward bias reduces as expected. The current density profiles for $L_d=5$ and 20 μm are shown in Fig. 4.15. As we can see from the 5 μm drift region case, with a high nominal current density of 6616 A/cm^2 @ 6 V, the current spreading is almost negligible: the effective current carrying diode width d_3 is found to be 72 μm , which corresponds to a current spreading width or length of only 1 μm at each side. On the other hand, when $L_d=20 \mu\text{m}$, the nominal current density reduces to 3215 A/cm^2 @ 6 V, the current spreading length is about 20 μm at each side. So we can see the current spreading length is strongly dependent on the current density.

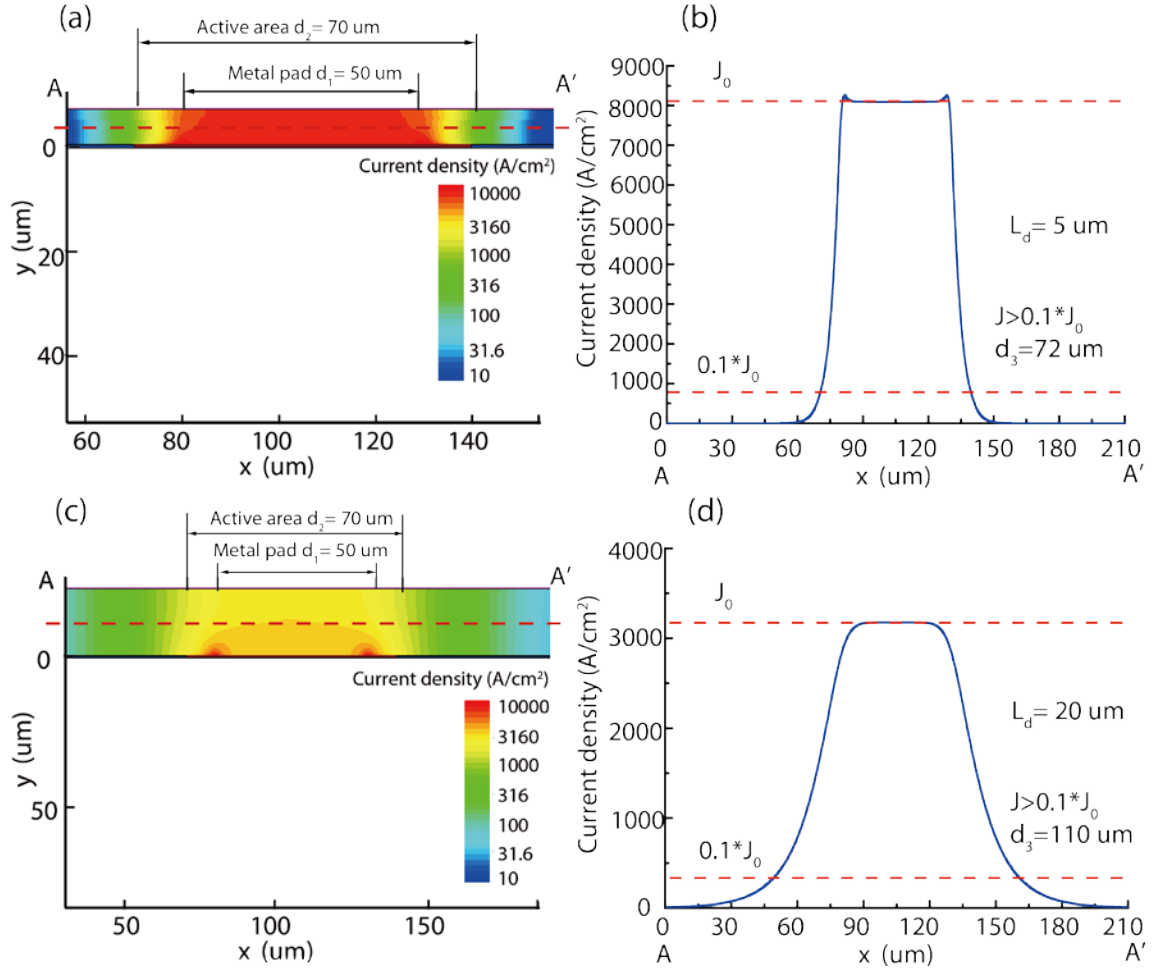


Figure 4.15 (a) Map of simulated current density of the GaN p-n diode with a drift layer thickness $L_d = 5 \mu\text{m}$, where a high current density of 6616 A/cm^2 (normalized to the diode mesa width) is reached at 6 V. (b) Current density profile across the middle of drift region of the $5 \mu\text{m}$ drift region diode. (c) Map of simulated current density of the GaN p-n diode with a drift layer thickness $L_d = 20 \mu\text{m}$, where a high current density of 3215 A/cm^2 (normalized to the diode mesa width) is reached at 6 V. (d) Current density profile across the middle of drift region of the $20 \mu\text{m}$ drift region diode.

For the electroluminescence (EL) measurement, the device we measured has a diameter of $417 \mu\text{m}$ at the bottom of the mesa. When the p-n junction device was biased at $J = 212 \text{ A/cm}^2$, we observed very low yellow luminescence (YL) around 2.3 eV as shown in Fig. 4.16, which is widely believed to be associated with carbon in the

n-type GaN films [88]. This low YL level indicates low carbon in the drift layer thus a high quality epitaxy. For the blue luminescence (BL) peak around 2.83 eV, this peak is associated with the electron-hole recombination from a deep donor state to the Mg acceptor state [89].

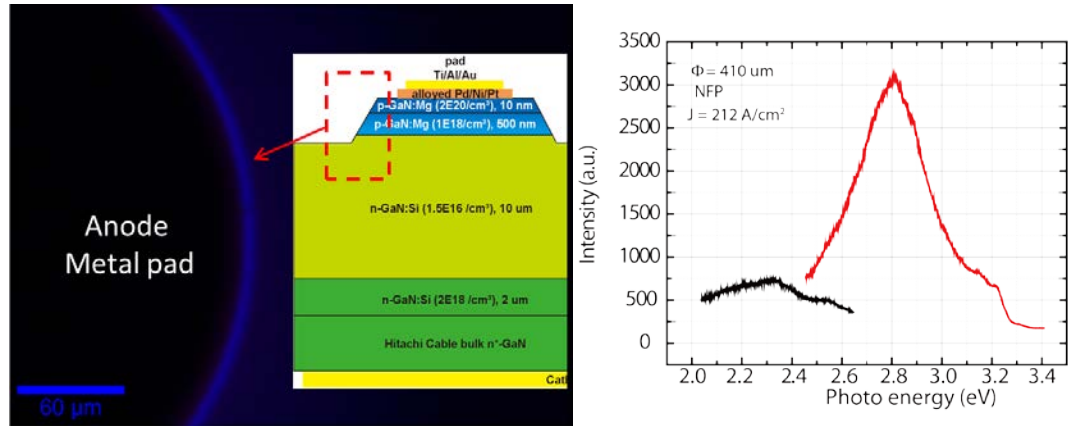


Figure 4.16 Electroluminescence image showing the blue light emission from the p-n diode mesa edge. The EL spectrum at an injection current level of 212 A/cm² (normalized to the diode mesa size) is shown at the right hand side, where the red curves shows the blue light with a peak at ~2.8 eV and some yellow light with a peak at ~2.2 eV is also seen. (Courtesy of Rusen Yan for EL measurement)

When the p-n junction device was biased at a higher current density $J = 341 \text{ A/cm}^2$, we carried out a space-resolved electroluminescence spectroscopic measurement as shown in Fig. 4.17. The distance from the edge of the anode metal of the p-n diode is varied from 0 to 25 μm , the EL spectra are collected and shown in Fig. 4.18. When the scanned distance increases from 0 to 5 μm , there is no significant change in the EL spectra, all showing 3 prominent EL peaks corresponding to the deep donor-Mg transition ($\sim 2.8 \text{ eV}$), shallow donor-Mg transition ($\sim 3.2 \text{ eV}$) and GaN band edge excitonic transition ($\sim 3.4 \text{ eV}$). When the distance increases to 10 μm , we observed a sharp decrease of the intensity of the EL signal although a faint blue emission (~ 2.8

eV) is still visible. The EL intensity and spectra are the same without detectable emission at 2.8 eV when measured at 15, 20 and 25 μm away from the diode mesa edge, suggesting this EL should arise from the n-GaN region (no EL peaks associated with Mg) but its spatial distribution might be partly complicated by light scattering and trapping within the sample. Nonetheless, this measurement provides us a first-order estimate of the current spreading within n-type region drift layer to be within 10 μm . A more careful analysis and modeling is necessary to extract further information.

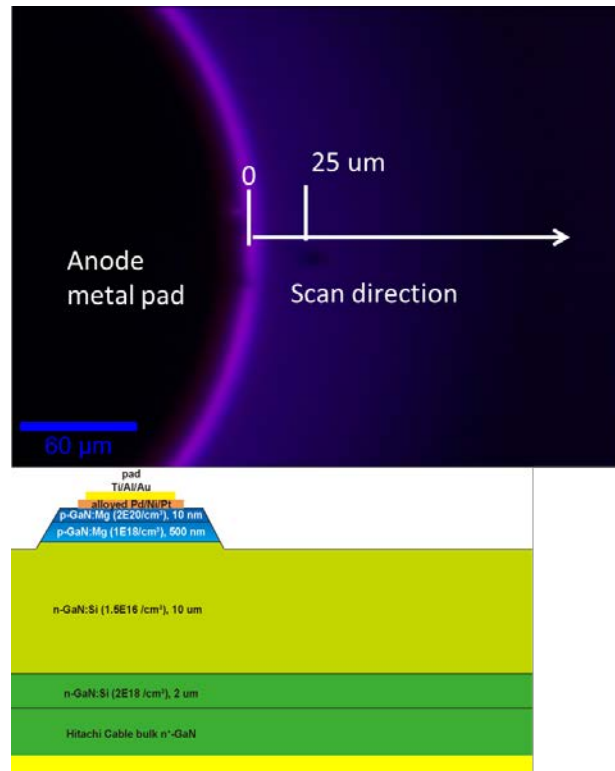


Figure 4.17 Space-resolved electroluminescence measurement setup. The white arrow show the scan direction. The zero point is at the edge of the diode anode metal contact, then the sample relative to the EL collection optical aperture is moved laterally 2 to 25 μm away. (Courtesy of Rusen Yan for EL measurement)

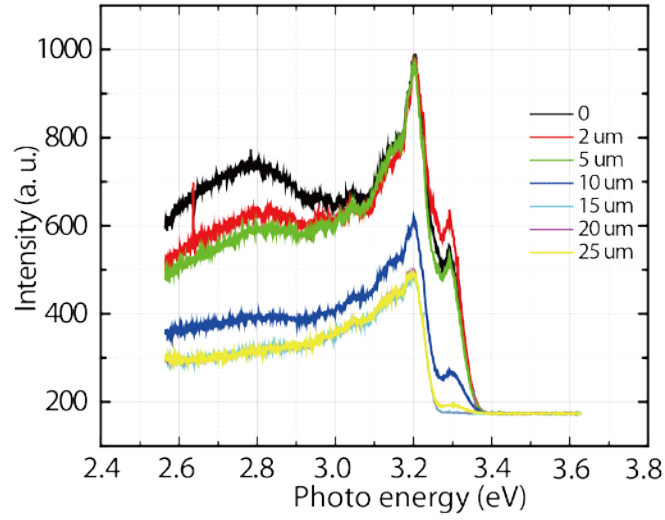


Figure 4.18 The EL spectra at an injection current level of 341 A/cm^2 at different locations, a dramatic decrease in intensity happens between 5 to $10 \mu\text{m}$ away from the anode edge. No significant variation in EL is observed between $15 \mu\text{m}$ and $25 \mu\text{m}$. (Courtesy of Rusen Yan for EL measurement)

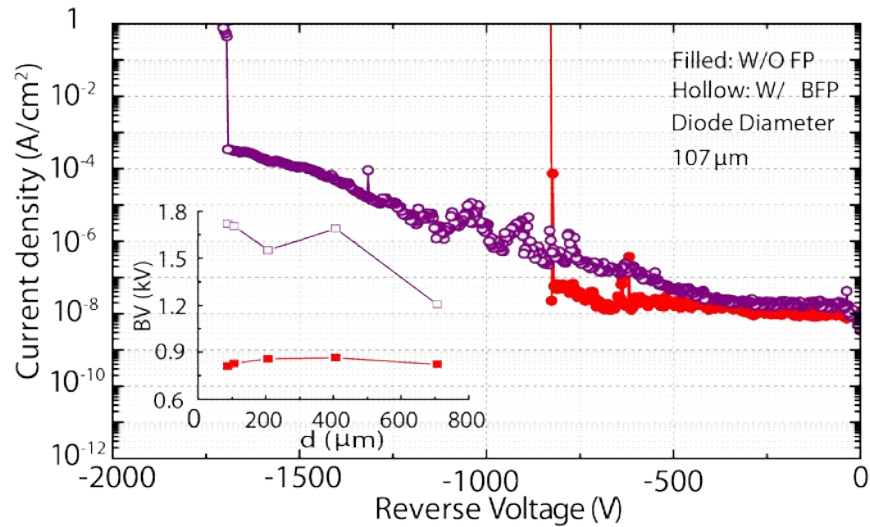


Figure 4.19 Reverse I - V characteristics of GaN p-n diodes w/ and w/o FP [81].

Based on the simulations and the spatial mapping of the EL shown above, we can estimate the degree of the current spreading in the diode shown in Fig. 4.10. For a forward bias $> 5.5 \text{ V}$, the diode current density is high, $> 4000 \text{ A/cm}^2$; considering a

maximum radius increase by 10 μm due to current spreading, an effective diode diameter is thus 127 μm and the corresponding R_{on} is calculated to be $0.55 \text{ m}\Omega\cdot\text{cm}^2$. Using the TLM and Hall effect measurements on the p-GaN, the GaN substrate resistance and assuming an electron mobility of $1000 \text{ cm}^2/\text{V}\cdot\text{s}$ and a lateral current spreading of 10 μm in radius in the n-GaN drift layer, all these resistance components sum up to be $0.64 \text{ m}\Omega\cdot\text{cm}^2$, which is slightly higher than the experimental value. The difference may be attributed to the underestimated electron mobility [90] or conduction modulation in p-n diodes[91], [92], demanding further studies.

Figure 4.19 shows the reverse I - V characteristics of the GaN p-n junction diodes w/ and w/o FP at room temperature, measured using an Agilent B1505A power device analyzer with devices covered by Fluorinert. For diodes w/o FP, BV is $\sim 830 \text{ V}$, showing a destructive failure near the mesa edge. For devices with FP, BV almost doubles, reaching 1706 V in diodes with a diameter of 107 μm . A slightly higher leakage at a higher reverse bias ($> 500 \text{ V}$) is most likely due to leakage path introduced by the FP process. The combination of BV of 1706 V and R_{on} of $0.55 \text{ m}\Omega\cdot\text{cm}^2$ leads to a high Baliga's figure of merit (V_B^2 / R_{on}) of $\sim 5.3 \text{ GW}/\text{cm}^2$ while taking into account of current spreading ($\sim 7.2 \text{ GW}/\text{cm}^2$ if the diode mesa size is used instead). This confirms that the field plate effectively suppresses the electric field crowding at the edge. It is interesting to notice in the inset of Fig. 4.18 that the BV of devices w/o FP are nearly independent of the diode size while that of the devices with FP decreases with increasing diode diameter. This observation indicates that the dislocations present in these diodes (about 100/5,000 total in the 107/707 μm diodes) might be tolerable in delivering kV devices.

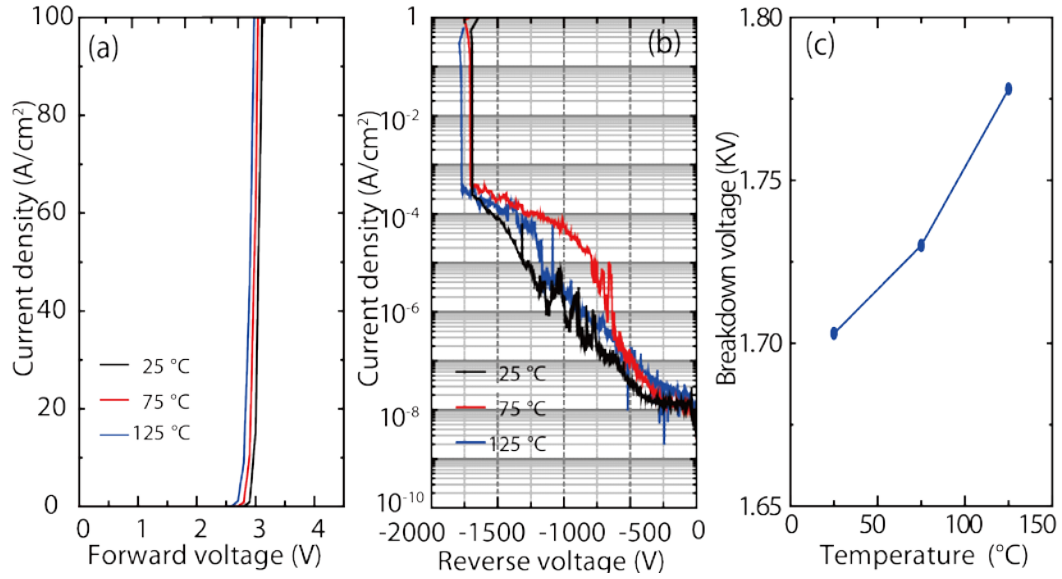


Figure 4.20 (a) Forward, (b) reverse I - V characteristics and (c) BV as a function of temperature, all obtained on the same device, which can be measured repeatedly. The origin of the abnormal leakage current at 75 °C is yet unclear [81].

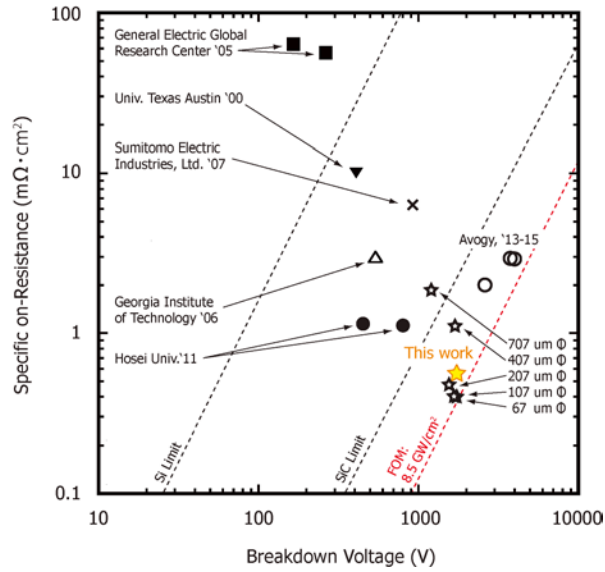


Figure 4.21 Benchmark plot of BV versus R_{on} in reported GaN p-n diodes. The solid star is the result obtained in diodes with an effective diode diameter of 127 μm taking into account of the effect of current spreading. The hollow stars are the results using the diode mesa bottom-diameter to calculate R_{on} . The dotted lines are the unipolar limit, where a mobility of 1100 cm^2/Vs and E_c of 3.4 MV/cm are used for GaN [81].

For an n-GaN drift layer with a thickness W of 10 μm and a net doping concentration $N_D - N_A$ of $1.2 \times 10^{16} \text{ cm}^{-3}$, the BV and E_C of an ideal planar junction in this punch-through structure are related by

$$BV = E_c W - \frac{q(N_D - N_A)W^2}{2\epsilon_s} \quad (4.9)$$

Since it is impossible to reach the ideal breakdown of a planer junction without employing an ideal edge termination, we estimate the critical electric field using the same criteria reported in Ref. [29]. Assuming 75% of the entitled breakdown voltage is achieved in our devices, the critical electric field E_C is estimated to be $> 3.5 \text{ MV/cm}$, which is among the best of the reported GaN devices [29], [87], [93], [94].

Figure 4.20 shows the temperature dependent characteristics of the 107 μm GaN p-n diode with FP. The forward turn-on voltage decreases with increasing temperature due to the exponentially increasing diffusion current with temperature. BV is observed to increase from $\sim 1706 \text{ V}$ at 25°C to 1778 V at 125°C , a signature of avalanche breakdown. The R_{on} - BV benchmark plot for the reported GaN p-n diodes is presented in Fig. 4. 21. Similar to Ref. [95], a diode-size dependent R_{on} is observed, which merits further investigation.

4.2.1.3 On-Wafer Reverse Recovery Time Measurement of GaN p-n Diodes

In high-voltage bipolar devices, the minority carrier lifetime is crucial to determine the conduction modulation, thus the maximum current density capability, as well as the reverse recovery time during switching, which contributes to the switching loss and ultimately limits the operating frequency of the device. For high-frequency switching applications, a short minority carrier lifetime is preferred since it facilitates

fast carrier recombination. In low-frequency and high-current/power applications, a long minority carrier lifetime is often desired since it takes advantage of the conduction modulation that can substantially lower R_{on} . With the development of SiC and GaN power devices, high-frequency power switching is emerging since it can improve the efficiency and also shrink the total size of the system by effectively reducing the passive components such as capacitors and inductors.

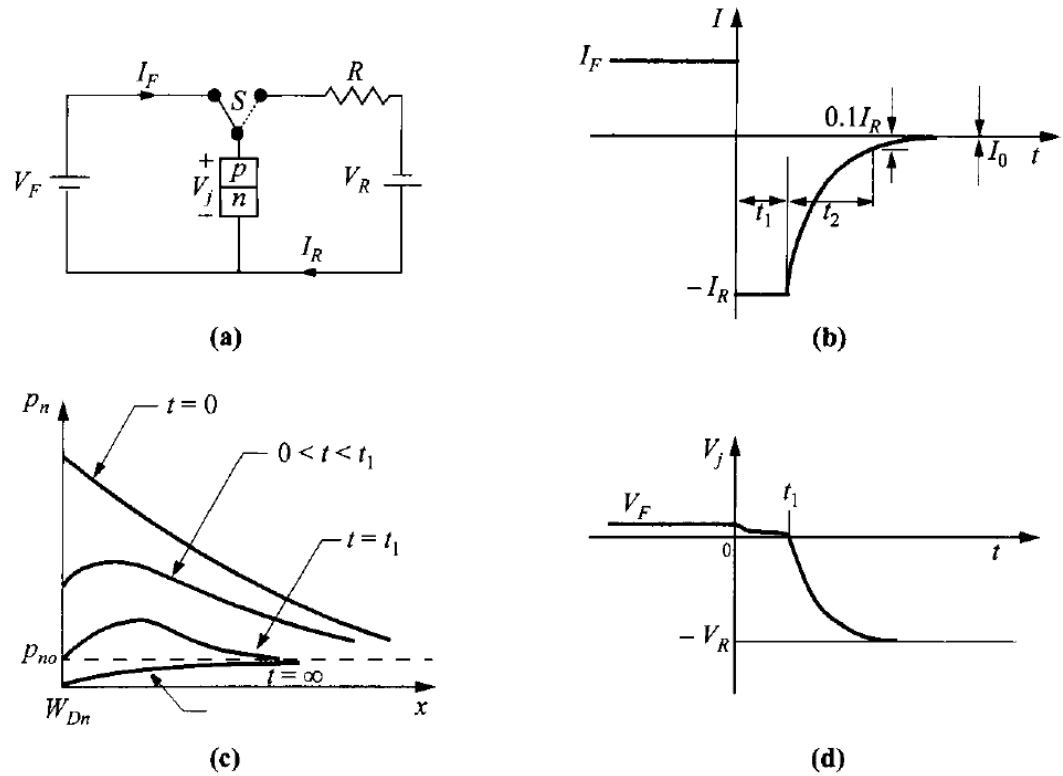


Figure 4.22 Transient behavior of a p-n junction: (a) the basic switching circuit, (b) the transient current response, (c) the minority-carrier distribution outside the depletion edge at various time intervals, and (d) the transient junction-voltage response[96].

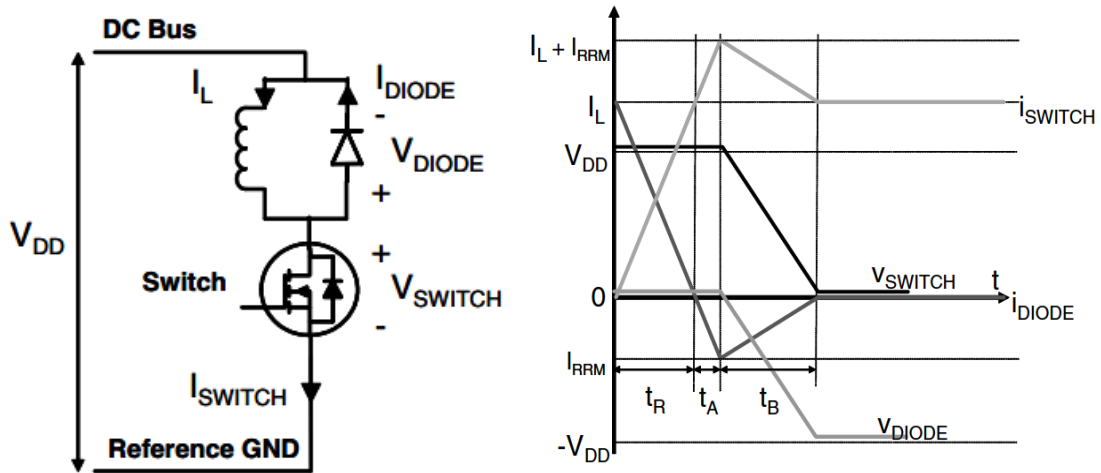


Figure 4.23 A typical circuit to measure the effect of diode reverse recovery and the diode current waveform [97]

One way to measure the minority carrier lifetimes is the reverse recovery time measurement of p-n diodes. Fig. 4.22(a) shows a conventional measurement scheme. The p-n diodes are first forward biased at I_F , thus there is injection and storage of minority carriers as shown at $t = 0$ s in Fig. 4.22 (c). When $t > 0$ s the devices is reverse biased at $I_R = (V_R - V_F)/R$; because there are excessive minority charges stored, it takes additional time for the carriers to recombine before it can start to turn off as shown in Fig. 4.21 (c). The transient time is defined as the time that the current drops to 10% of the initial reverse current I_R , which is the sum of the charge storage time t_1 and current decay time t_2 in Fig. 4.22(b). The resulting current and voltage waveform are shown in Fig. 4.22(b) and (d), respectively. Fig. 4.23 shows a typical circuit to test the diode reverse recovery time and the diode current waveform from the circuit. For this kind of measurements, it typically requires complex circuits and packaged devices, which demands additional circuit board design and packaging time and effort. Thus a quick on-wafer reverse recovery time measurement for easy and

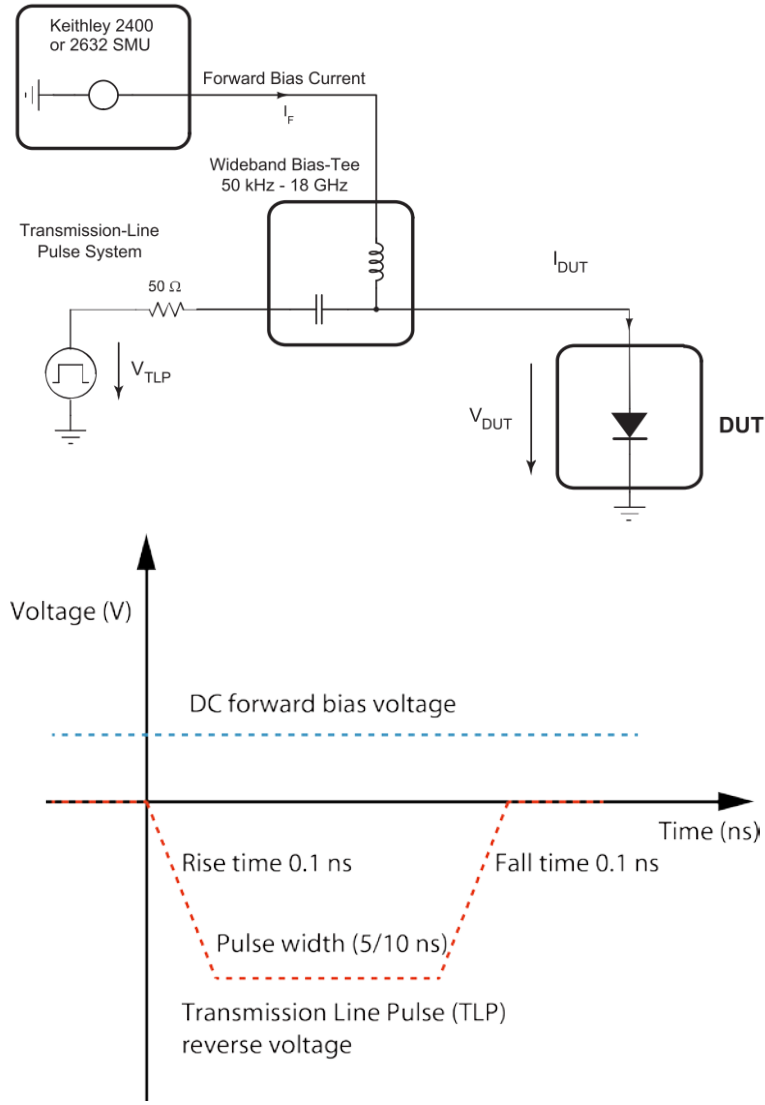


Figure 4.24 On-wafer reverse recovery time measurement setup using a TLP system from HPPI, a SMU is used for DC power supply to provide forward voltage bias. Lower panel is the schematic of the applied voltage DC and pulse voltage waveforms [98], [99]. The TLP pulse can have a pulse width ranging from 5 ns to 100 ns. The rise and fall time of the pulse is about 0.1 ns.

quick evaluations is highly desirable. Besides, GaN is a direct bandgap material, which is different from indirect bandgap materials such as Si and SiC. Thus the minority carrier lifetime of GaN would be substantially lower than that of Si and SiC, and it also results in more challenges for the accurate measurement of the minority

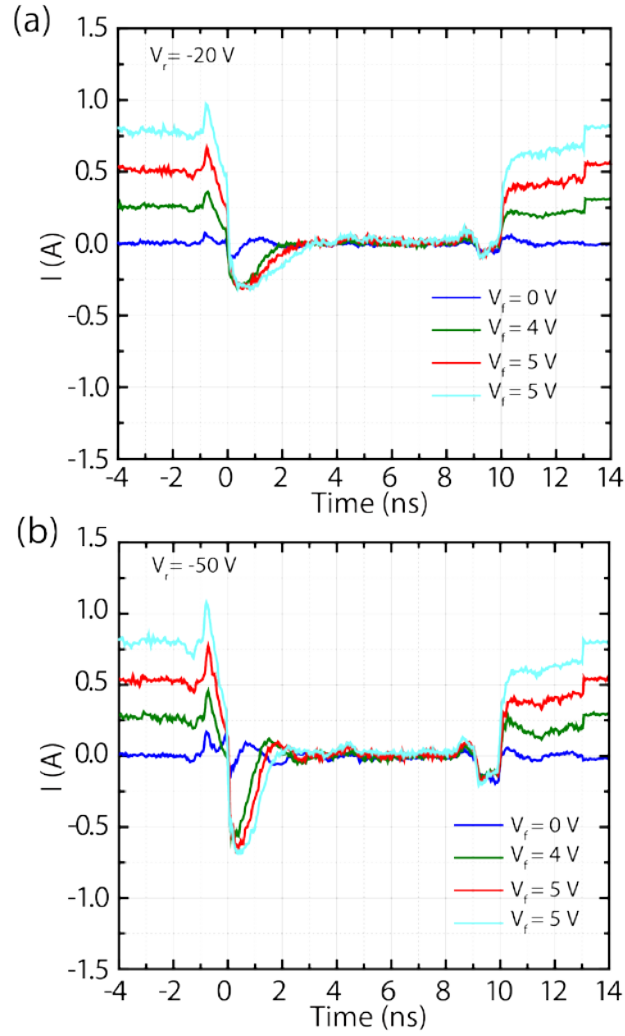


Figure 4.25 Current waveforms obtained during the reverse recovery measurement of the p-n diodes shown in Section 4.1.2 under a pulsed reverse voltage V_r of -20 V and -50 V with a 10 ns pulse width and various forward voltages V_f .

carrier lifetime in GaN. To address these two problems, we use a transmission line pulsing (TLP) system in collaboration with Analog Devices Inc., which is capable to generate high voltage pulse up to 1500 V with pulse width from 5 to 200 ns and rise/fall time of 0.1 ns. The TLP system is used to generate the high voltage reverse voltage pulse while a DC power supply (SMU in this case) is used to turn on the device for forward current conductions and minority carrier injections. The schematic

diagram of the test system is shown in Fig. 4.24(a) and the applied waveform is shown in Fig. 4.24 (b). The device under test has a radius of 407 μm . The measured current waveforms with a pulse width of 10 ns are shown in Fig. 4.25 at various forward voltages $V_f=0, 4, 5, 6$ V and various reverse voltage $V_r = -20$ and -50 V. Since the current is obtained by subtracting the incident current from the reflection current, the current overshoots between ~ -1 to 0 ns and ~ 9 to 10 ns are due to misalignment of the incident current and the reflection current. So we can see there is a current overshoot when $V_f = 0$ V. It is found from the waveforms that the diode can be fully turned off within ~ 2 ns for a forward current injection up to 0.8 A. When comparing the diodes at different forward voltage V_f values (a higher current/minority carrier injection at a higher V_f), we found that it takes a longer time for the p-n diodes to fully turn off at a higher V_f as shown in Fig. 4.25(a). This longer reverse recovery time is expected since it needs more time for the recombination process to remove the excessive minority carriers. When we increase the reverse voltage from -20 to -50 V, the reverse recovery time reduces to be smaller than 2 ns as shown in Fig. 4.25(b). Since the devices can be turned off in about 2 ns, we also used a pulsed reverse voltage with a 5 ns pulse width to measure the reverse recovery process and the results are shown in Fig. 4.26. From the current waveforms, similar conclusions can be made in terms of the reverse recovery time compared to the case using a 10 ns pulse width. Fig. 4.27 shows the current waveforms obtained during the reverse recovery measurement with a 5 ns pulse width under different V_r from -20 to -100 V but at a fixed $V_f : 5$ V and 6 V. It clearly shows that the reverse recovery time reduces with a higher reverse voltage.

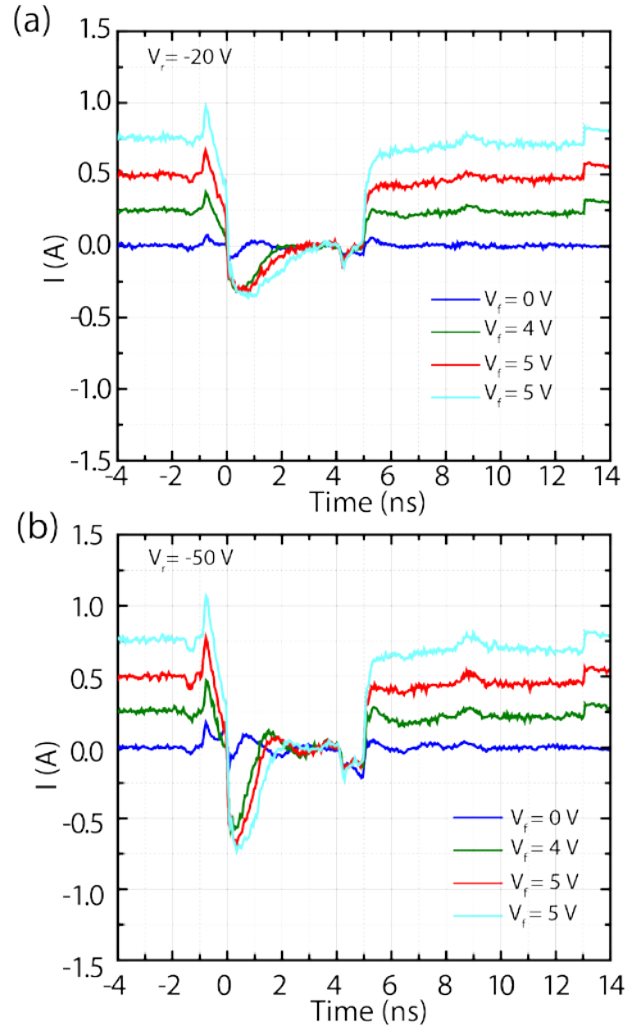


Figure 4.26 Current waveforms obtained during the reverse recovery measurement under a pulsed reverse voltage V_r of -20 V and -50 V with a 5 ns pulse width and different forward voltages.

We also compare the devices W/ and W/O field plate as shown in Fig. 4.28. No significant difference has been observed, which indicates the reverse recovery time is dominated by the intrinsic junction performance rather than the parasitic RC charging.

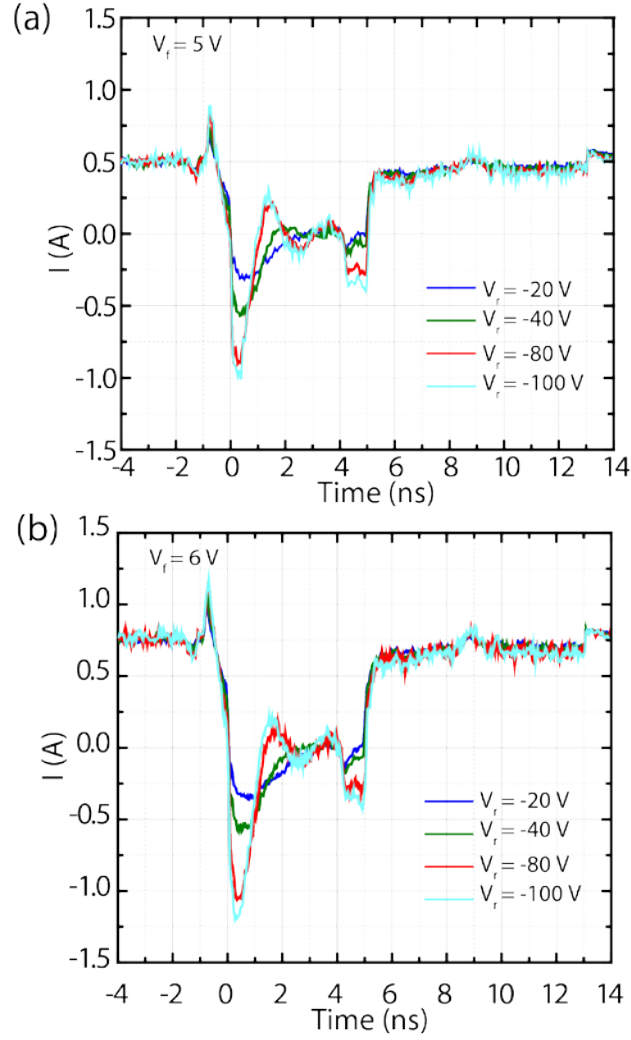


Figure 4.27 Current waveforms obtained during the reverse recovery measurement with a 5 ns pulse width under different V_r but at a fixed V_f of (a) 5 V and (b) 6 V.

Since we did not observe a significant charge storage time (i.e. a plateau in the reverse current in the waveforms), we use the total reverse recovery time for the current decay phase to extract the hole minority life time, which can be expressed as [96]

$$\text{erf}(\tau_{rr} / \tau_p) + \frac{\exp(-\tau_{rr} / \tau_p)}{\sqrt{\pi \tau_{rr} / \tau_p}} = 1 + 0.1 \left(\frac{I_R}{I_F} \right) \quad (4.10)$$

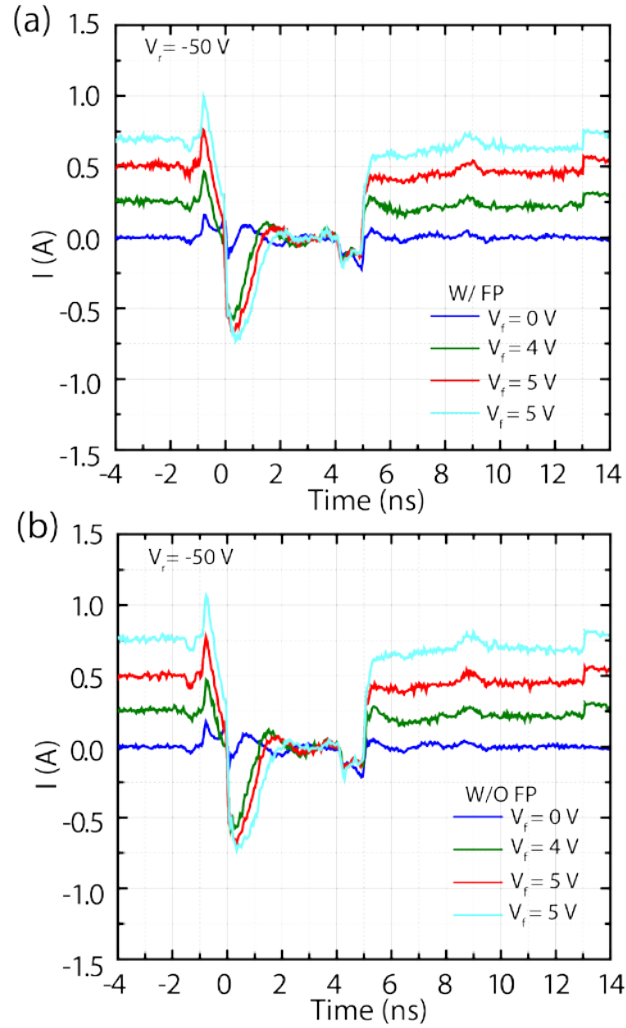


Figure 4.28 Current waveforms obtained during the reverse recovery measurement with a 5 ns pulse width under different V_f but at a fixed V_r for devices (a) W/O FP, and (b) W/ FP.

From this equation, we can extract the τ_{rr} / τ_p as a function of I_R / I_F as plotted in Figure 4.29(b). Since we also know τ_{rr} at different I_R / I_F , we can extract the hole minority carrier lifetime τ_p to be ~ 2.3 ns. This extracted hole minority carrier lifetime is slightly higher than the reported hole lifetime of ~ 0.7 - 0.8 ns in n-GaN with

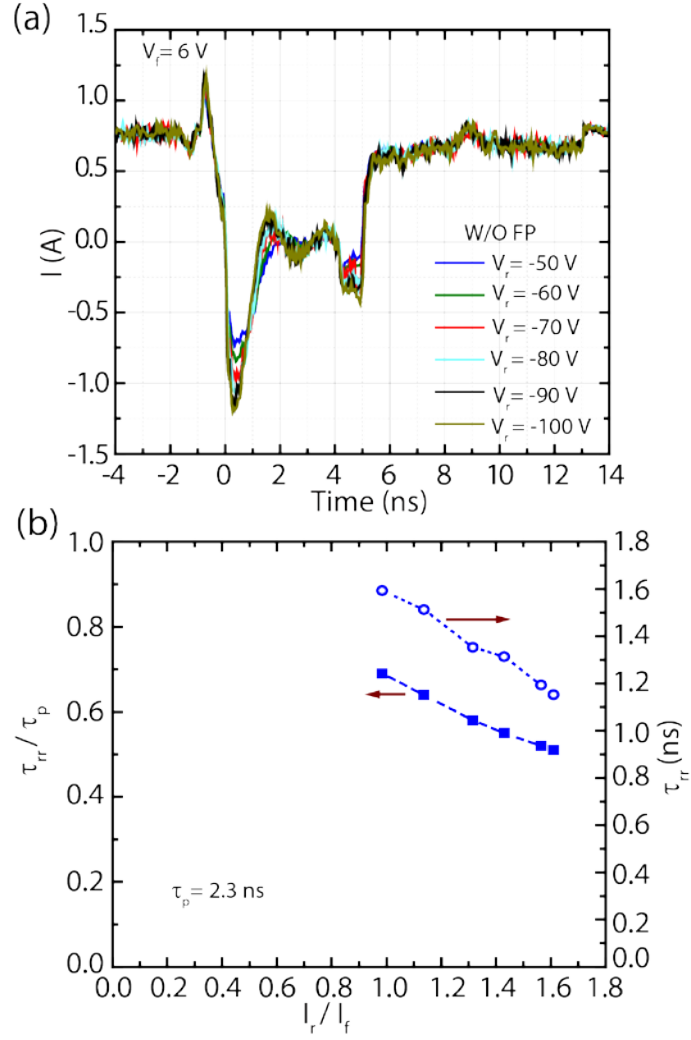


Figure 4.29 (a) Different reverse recovery characteristics at different reverse voltages V_r for the same V_f/I_f on a 410 μm diode without FP. (b) The corresponding minority hole lifetime extracted from the total reverse recovery time.

a doping concentration of $4 \times 10^{17} - 4 \times 10^{18} \text{ cm}^{-3}$ [100], which may be attributed to the high quality n-GaN drift region with a low doping concentration of $\sim 4 \times 10^{17} \text{ cm}^{-3}$ grown on high-quality GaN substrates with low defect densities. Nevertheless, an ultra-low hole minority carrier lifetime indicates that GaN p-n diodes are suitable for high speed switching applications. On the other hand, it also indicates it will be challenging to realize GaN power devices for very-high-voltage applications ($> 5 \text{ kV}$)

with high current capabilities since the current conduction modulation in GaN would be significantly smaller compared to Si and SiC with a minority lifetime of few μs .

The textbook-like behavior in our GaN p-n power diodes, with avalanche capability demonstrated, which signifies the quality of epitaxial GaN is now on par with that of SiC while the performance and yield of large area power devices will most likely improve dramatically with further reduction of threading dislocations in bulk GaN substrates. On-wafer reverse recovery measurement shows the device can be switched off in about 2 ns and the extracted minority-carrier hole lifetime ~ 2.3 ns. Hence, this work places another landmark toward realizing true potentials of GaN-on-GaN for power electronics applications and set an excellent benchmarking example for our development of the *Pi-doped* power devices discussed in the next section.

4.2.2 Development of High-Voltage GaN Polarization-doped (Pi-doped) p-n Diodes

4.2.2.1 First Generation of Impurity and Pi-doped p-n Junction Devices

The development of *Pi-doped* GaN p-n junction diodes has been carried out using both MOCVD with IQE and molecular beam epitaxy (MBE) with Prof. Jena's group. While the MBE work has been recently documented in Meng Qi's Ph.D. dissertation, in this thesis the development using MOCVD epitaxial structures grown by IQE is described. The designed epitaxial structures for Impurity- and *Pi-doped* GaN p-n diodes for a target breakdown voltage of 1200 V are shown in Fig. 4.30(a) and (b). The Impurity-doped device structure is grown in each generation of the development, partly as control samples and partly to monitor the epitaxial quality. The impurity doped p-n junction consists of a 8 μm drift region with a Si doping of $2 \times 10^{16} \text{ cm}^{-3}$ and a 0.4 μm p-type region with a Mg doping of $1 \times 10^{19} \text{ cm}^{-3}$. For the *Pi-doped* GaN p-n

diodes, the drift region consists of a 7 μm impurity-doped drift region with a Si doping of $2 \times 10^{16} \text{cm}^{-3}$ and 1 μm *Pi-doped* layer realized by grading the Al composition from GaN linearly to $\text{Al}_{0.05}\text{GaN}$; the p-type layer is formed by linearly grading AlGaN back to GaN over a thickness of 0.4 μm . A Mg doping of up to $1 \times 10^{19} \text{cm}^{-3}$ is added in the p-type layer to overcome the effect of compensation centers. After the epitaxy growth of the GaN device wafer, the similar processes as described in section 4.2.1 are used to fabricate p-n diodes.

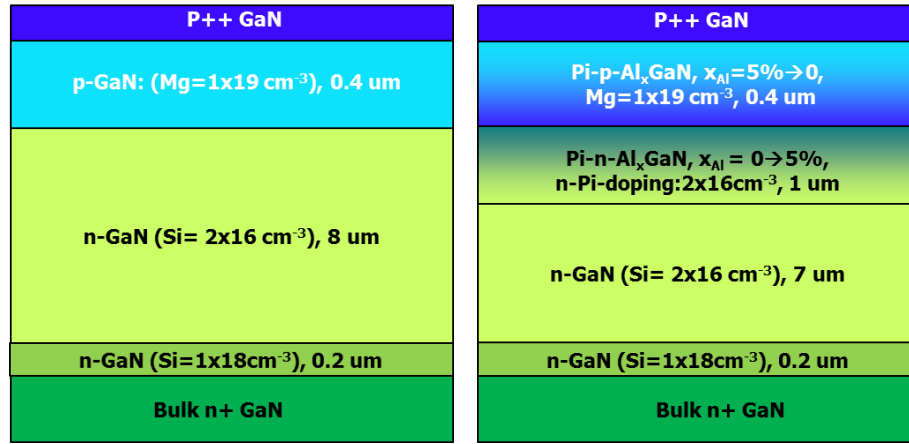


Figure 4.30 Epitaxial structure of (a) Impurity doped and (b) Pi-doped GaN p-n diodes.

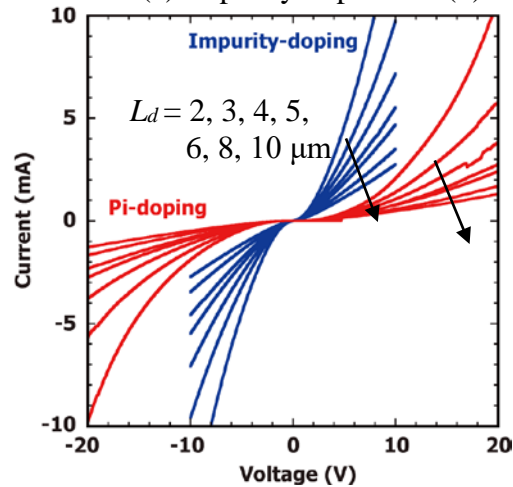


Figure 4.31 TLM I - V curves of the top p-ohmic contacts with a gap varied from 2 to 10 μm and a contact width of 50 μm (Courtesy of Dr. Kazuki Nomoto).

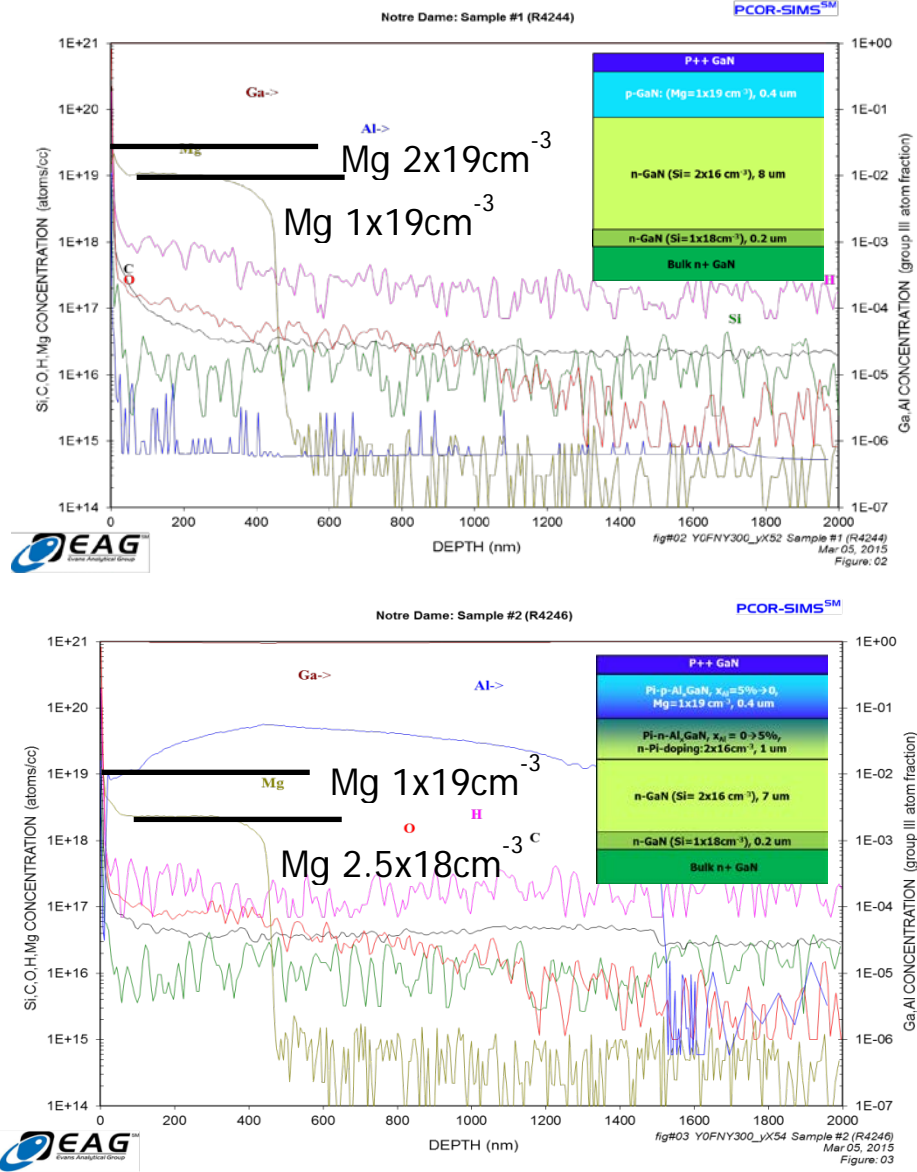


Figure 4.32 SIMS profiles in the first generation (a) impurity-doped and (b) Pi-doped GaN p-n junction epitaxial layers (SIMS from EAG).

On the fabricated devices (fabrication by Dr. Kazuki Nomoto), the top p contacts with different gap sizes from 2 to 10 μm are measured and shown in Fig. 4.31. For a pair of contacts with a 2 μm gap distance, in the *Imp-doped* p-n diodes the current reaches 10 mA at 8 V, which is significantly higher than that in the *Pi-doped* device at ~20 V. Meanwhile, the p-contact *I-V* shows severely non-linear *I-V* characteristics in

Pi-doped devices than the nearly ohmic characteristics observed in the impurity-doping ones. When we compare the SMIS results of these two devices as shown in Fig. 4.32, we find that the Mg doping level in the impurity-doped epi is higher than that in the *Pi-doped* one, both in the p++ GaN layer (2×10^{19} vs 1×10^{19} cm⁻³) and the p-GaN layer (1×10^{19} vs 2.5×10^{18} cm⁻³). Since the lower Mg doping in the p++ GaN region would lead to a lower acceptor concentration, which consequentially lead to poorer ohmic contacts.

4.2.2.2 First-Generation-Diode DC Characteristics

The representative forward and reverse *I-V* characteristics of the impurity and *Pi-doped* GaN p-n junction diodes with and without FP at *room temperature* is shown in Fig. 4.33(a) and (b), respectively. We can see normal *I-V* characteristic in the impurity-doped devices, while an abrupt jump in the forward *I-V* near 3 V for the *Pi-doped* device. For the reverse characteristics shown in Fig. 4.33(b), diodes with beveled field plates (BFP) and a diameter varied from 67 to 207 μ m are measured; both impurity and *Pi-doped* diodes achieved low leakage below 1×10^{-7} A/cm² up to 1100 V. The breakdown voltages of the *Pi-doped* devices are around 1346 V, which is slightly higher than 1322 V observed in the impurity-doped ones.

The temperature dependent characteristics for both diodes are shown in Fig. 4.34. Impurity-doped p-n diodes *I-V* curves show the turn-on voltage slightly decreases with temperature, which is the same trend as the previous benchmark impurity p-n diode. While for the *Pi-doped* p-n junction, since there are abrupt jumps in the currents at different temperatures, there is no clear trend in terms of the turn-on voltage. For the

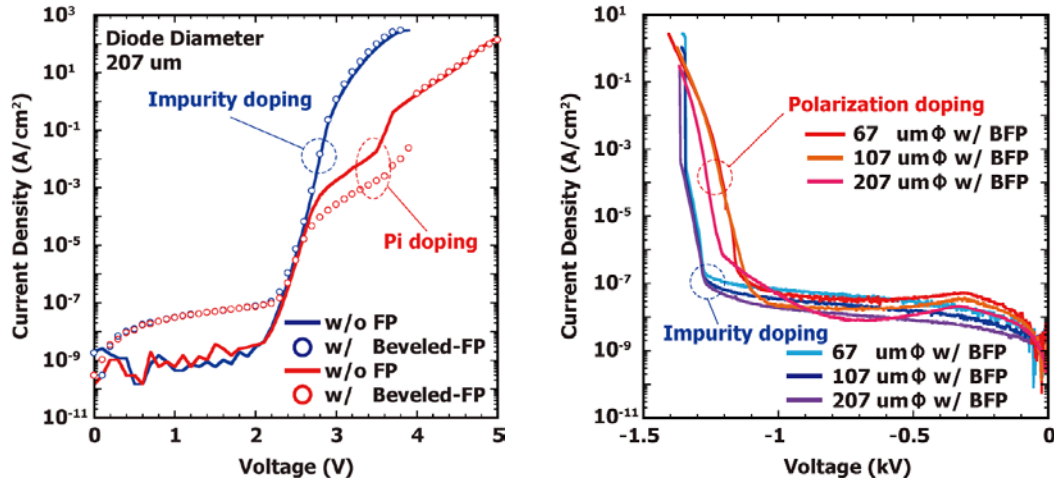


Figure 4.33 (a) Forward and (b) reverse I - V characteristics of the first generation impurity and Pi-doped GaN p-n diodes at room temperature.

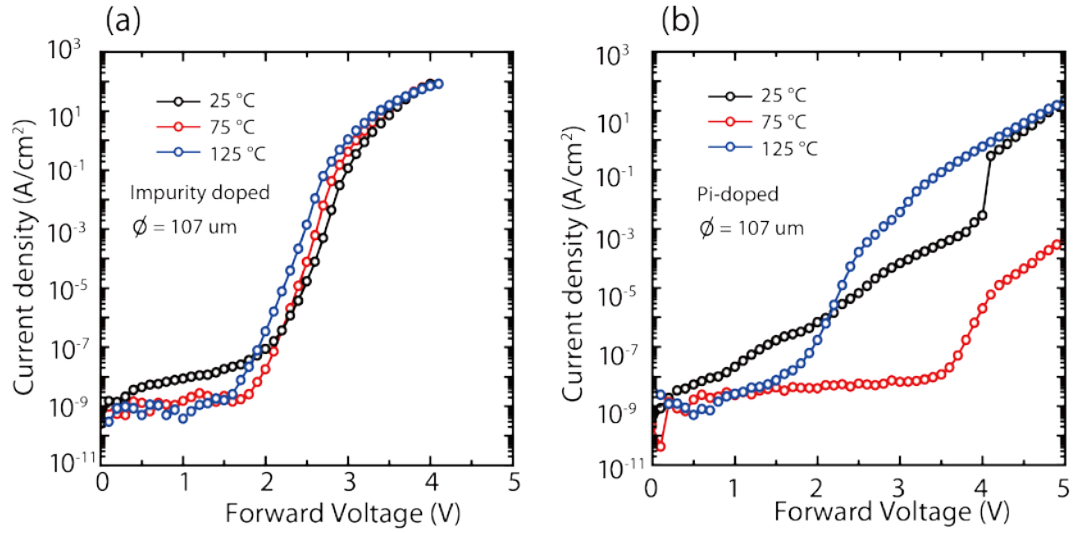


Figure 4.34 Forward I - V characteristics of (a) impurity and (b) Pi-doped GaN p-n diodes with a diameter of 107 μm at different temperatures up to 125 $^{\circ}\text{C}$.

reverse biased conditions, both devices show that the off-state leakage increases with higher temperature. While the breakdown voltage of impurity-doped p-n diode shows a positive slope with increasing temperature (1322 V@ 25 $^{\circ}\text{C}$ vs 1408 V @125 $^{\circ}\text{C}$),

the *Pi-doped* p-n diode shows a decreasing breakdown voltage from 1346 V to 1320 V when the temperature increasing from 25 to 125 °C.

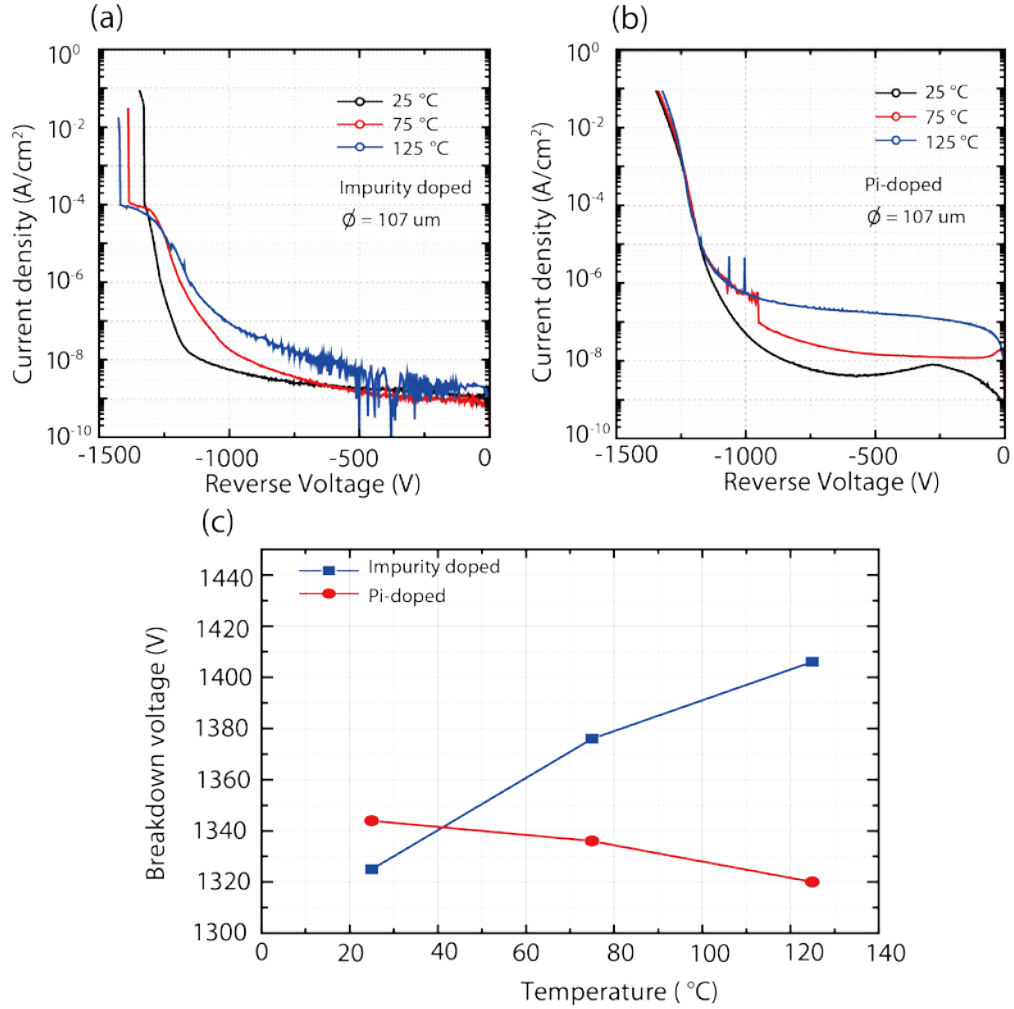


Figure 4.35 Reverse *I-V* characteristics of (a) impurity and (b) *Pi-doped* GaN p-n diodes with a diameter of 107 μm at different temperatures up to 125 °C. (c) Summary of breakdown voltage change with increasing temperature up to 125 °C, Impurity doped GaN p-n diodes breakdown voltage increases with temperature, while *Pi-doped* GaN p-n diodes breakdown voltage decreases with increasing temperature.

To better understand the significant differences, we did *C-V* measurements for both diodes with a diameter of 409 μm at 100 kHz as shown in Fig. 4.36. For impurity-

doped p-n diodes, the C - V shows good modulation of the capacitance by applying a voltage. The extracted net electron concentration profile from the junction in the n-GaN drift region is shown in Fig. 4.36(b), where $N_D - N_A \sim 6\text{--}8 \times 10^{15} \text{ cm}^{-3}$ is obtained compared to a target of $2 \times 10^{16} \text{ cm}^{-3}$ by Si doping. This is consistent with the SIMS profile shown in Fig. 4.32 (a) where the overall Si doping concentration is higher than the C impurity concentration but the Si donor states can be appreciably compensated by the C acceptor states (C is believed to act as deep acceptor in GaN, will be discussed later). The built-in voltage V_{bi} extracted from C - V is $\sim 3.04 \text{ V}$, which is very close to the theoretical value of 3.21 V . Besides, the depletion depth at zero bias is $\sim 668 \text{ nm}$, comparable to the expected value of 653 nm . All these results indicate the impurity doped p-n diodes behave reasonably well to what we expected.

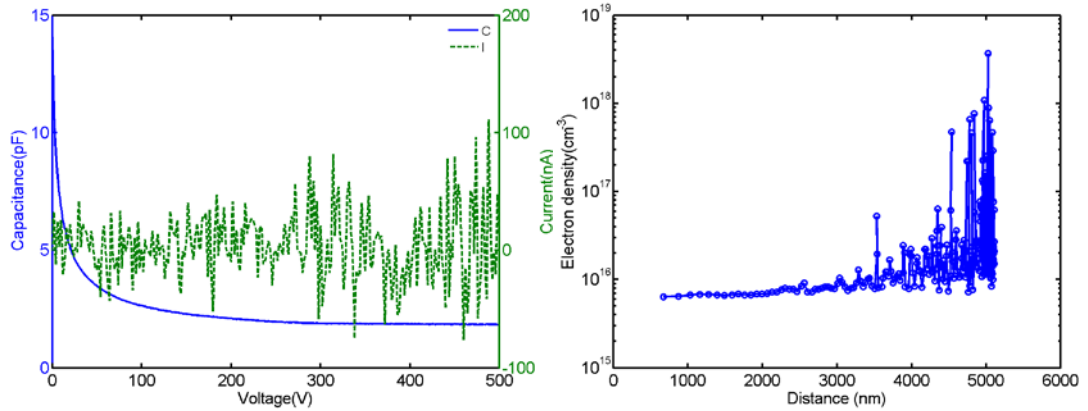


Figure 4.36 (a) C - V characteristics of impurity-doped GaN p-n diodes without FP and a diameter of $407 \mu\text{m}$ at 100 kHz , (b) Extracted net electron density profile from the C - V measurement.

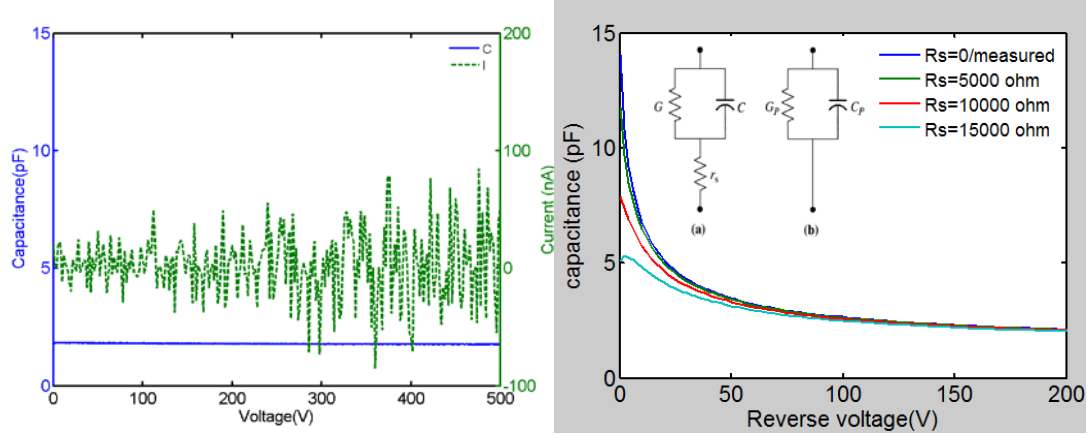


Figure 4.37 (a) C - V characteristics of Pi -doped GaN p-n diodes without FP and a diameter of $407\text{ }\mu\text{m}$ at 100 kHz , (b) Consider there is a series resistor with the capacitance and conductance network, which can lead to a lower apparent capacitance. However, even with a high series resistance of $15,000\text{ }\Omega$, the resulting zero voltage capacitance is $\sim 5\text{ pF}$, which is still larger than the measured zero voltage capacitance of the Pi -doped p-n diode of 2 pF . The abnormally small apparent capacitance most likely rises from a heavily compensated drift layer.

The *Pi*-doped p-n junction C - V results are shown in Fig. 4.37 (a), where the capacitance almost remains unchanged over the 500 V sweep. Besides, the capacitance at zero voltage bias is about 2 pF , which is much smaller than 14 pF for the impurity-doped p-n diode. It is possible that there are capacitances in series from the top non-ideal p-contact acting as Schottky contacts, which is evidenced by the non-linear I - V of the top contact TLM measurement. It is also highly possible that the low capacitance comes from the high series resistance from the n-drift region, with the model shown in the inset of Fig. 4.37 (b). Ideally the zero bias capacitance of these two diodes should be similar. The main difference we observed can be further explained by an additional series resistance. It can be found that a big resistance is needed to be in series with the capacitance and conductance network. With a resistor of $15,000\text{ ohm}$ in series, the zero bias capacitance reduces from 14 pF to $\sim 5\text{ pF}$. This

big resistance translates to a net electron concentration $\sim 1.8 \times 10^{10} \text{ cm}^{-3}$ for a drift region thickness of $5 \text{ }\mu\text{m}$ assuming an electron mobility of $\mu_n = 1000 \text{ cm}^2/(\text{V}\cdot\text{s})$. With this low electron concentration in the drift region, it means the drift region is highly compensated by the high C impurity incorporated as confirmed by the SIMS results (C concentration $\sim 3 \times 10^{16} \text{ cm}^{-3}$ vs Si concentration $\sim 1\text{--}2 \times 10^{16} \text{ cm}^{-3}$) in Fig. 4.32(b).

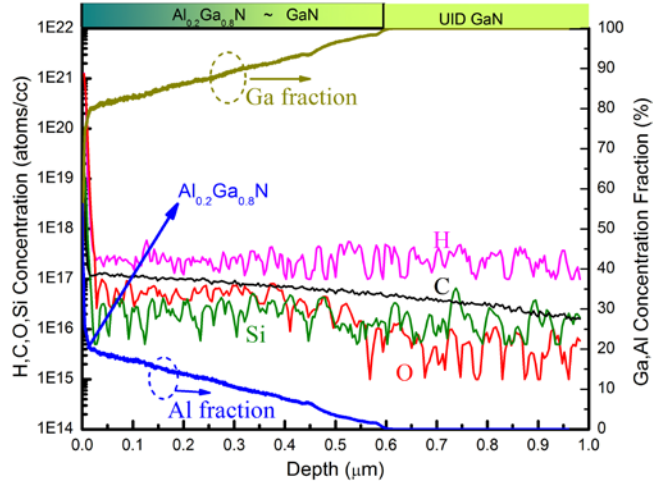


Figure 4.38 SIMS profile of a linearly graded layer from GaN to $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ over $0.6 \text{ }\mu\text{m}$ on UID GaN grown on sapphire substrate. The C impurity level is about $1 \times 10^{17} \text{ cm}^{-3}$. [Courtesy of Mingda Zhu]

The impact of C impurity incorporation in n-type GaN has been studied and the results suggest that it acts as deep acceptor [101],[102]. Recently, our group and Sandia National Lab also did Deep Level Optical Spectroscopy (DLOS) measurements on the *Pi-doped* layer to evaluate the effect of C on the *Pi-doped* layer. The structure consists of a linearly graded layer from GaN to $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ over $0.6 \text{ }\mu\text{m}$ on UID GaN on sapphire substrate. The layer structure and its associated SMIS results are shown in Fig. 4.38, where the C impurity level was revealed to be $\sim 1 \times 10^{17} \text{ cm}^{-3}$. The DLOS measurement spectra of the *Pi-doped* layer in Fig. 4.39 showed several

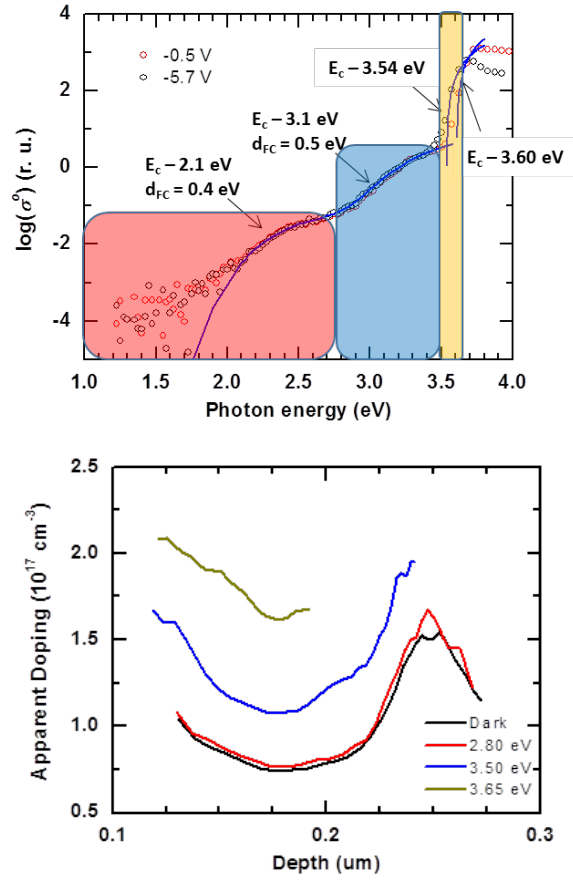


Figure 4.39 (a) DLOS measurement spectra for the Pi-doped layer on sapphire substrate, showing there are mainly three acceptor levels: $E_c-2.1$, $E_c-3.1$ and $E_c-3.54/4.60$ eV and (b) the extracted apparent doping profile for different photon energy measurement. [Courtesy of Dr. Armstrong Andrew at Sandia National Lab]

band-gap states: $E_c-2.1$, $E_c-3.1$ and $E_c-3.54/4.60$ eV. The apparent doping concentration for these three states is 2.5×10^{15} , 3.1×10^{16} , $5.7 \times 10^{16} \text{ cm}^{-3}$, respectively. The sum of these three state concentrations is about $9.05 \times 10^{16} \text{ cm}^{-3}$, which is very close to the C concentration from the SIMS results. This indicates that the C impurity also acts as deep acceptor in the *Pi-doped* layer. So for our *Pi-doped* and impurity doped n-drift layer in the Pi-dope p-n junction, since there is a higher C concentration than the Si concentration in the drift layer, it results in strong compensation. It also

may be linked to the abnormal forward I - V and reduced BV with increasing temperature, more detailed studied need to unveil the detailed relationship.

Table 4.1 Summary of the DLOS measurement of different energy levels and density [Courtesy of Dr. Armstrong Andrew at Sandia National Lab]

Energy level(eV)	Density(cm^{-3})
E_c -2.1	2.5×10^{15}
E_c -3.1	3.1×10^{16}
E_c -3.54/3.60	5.7×10^{16}

4.2.2.3 Second Generation Pi-doped p-n Junction Devices

Having identified the issue of heavy compensation in the drift region due to high levels of C impurity and the p-type ohmic contact problem associated with the low Mg doping level, a second batch of epitaxial growth was designed and carried out to tackle these problems.

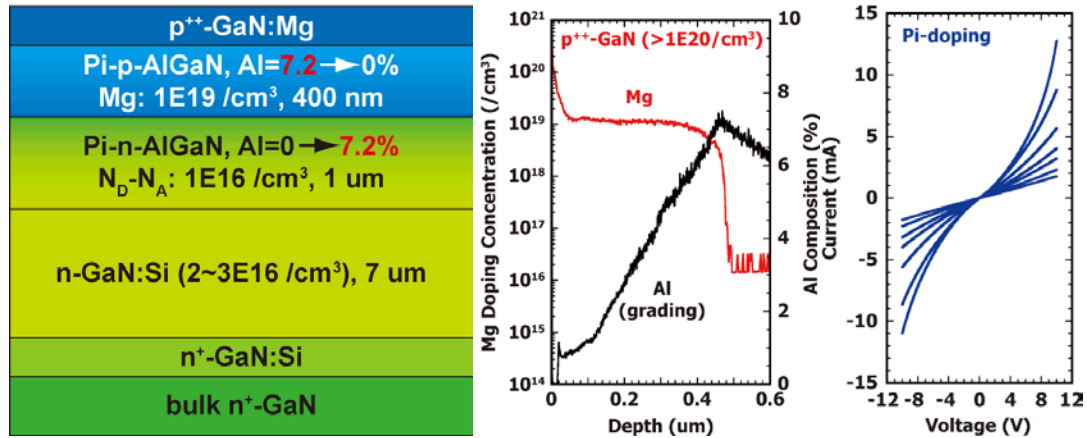


Figure 4.40 Epitaxial structures of *Pi-doped* GaN p-n diodes. SIMS results show the Al composition and Mg doping profiles in the top p^{++} GaN and p-GaN layer closely follow the designed profile. The TLM measurement shows good p-contacts. [Courtesy of Dr. Kazuki Nomoto]

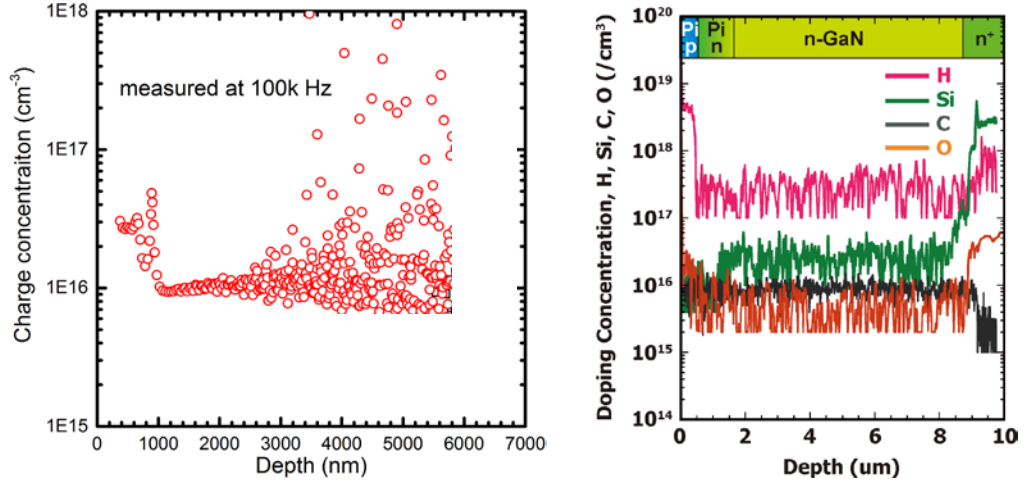


Figure 4.41 (a) Extracted net electron concentration profile for *Pi-doped* p-n junction at 100 kHz. (b) SIMS profiles of Si, C, H and O in the epitaxial layers. [Courtesy of Dr. Kazuki Nomoto]

The same epitaxial structure design shown in Section 4.2.2 is used for the growth with improved control of impurity incorporation and Mg doping. SIMS measurements are done after the growth, which shows the final Al composition is 7.2%. In Fig. 4.40 the epitaxial layer information is updated to better reflect the experimentally determined structures.

On fabricated devices (by Dr. Kazuki Nomoto), the top p-type TLM contacts with different gaps from 2 to 10 μm have been measured, which show good current capability and linearity. This is expected improvement since the top p++ GaN and p-GaN region has a high Mg doping of $>1 \times 10^{20} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$ as shown in the SIMS profile.

C-V measurement in Fig. 4.41(a) shows that the net electron density at the *Pi-doped* layer is about $3 \times 10^{16} \text{ cm}^{-3}$, which agrees well with the expected doping concentration by grading GaN to $\text{Al}_{0.072}\text{GaN}$ over 1 μm . The Si doping in the impurity-doped layer is about $2\text{-}3 \times 10^{16} \text{ cm}^{-3}$ as shown in Fig. 4.42(a). When we reduce the C impurity from

3×10^{16} in the first generation epitaxy to $1 \times 10^{16} \text{ cm}^{-3}$, below the Si doping level in the impurity-doped drift region, we can get a net electron concentration of $1 \times 10^{16} \text{ cm}^{-3}$, this further confirms the compensation effect of C in GaN.

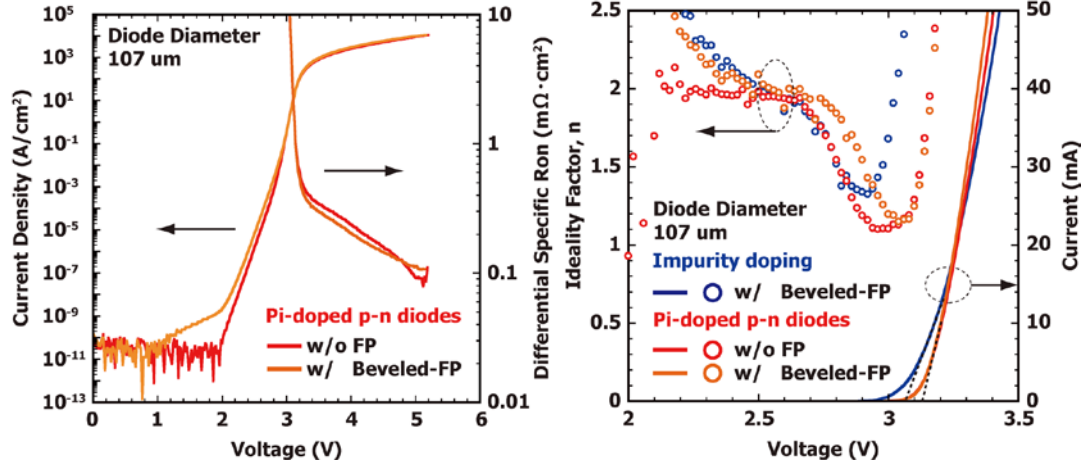


Figure 4.42 Forward I - V characteristics of $\text{Pi-doped GaN p-n junction diodes}$ w/ and w/o FP (a) in logarithm scale and R_{on} w/o considering lateral current spreading, and (b) in linear scale and the ideal factor of the diodes. [Courtesy of Dr. Kazuki Nomoto]

The forward I - V characteristics are shown in Fig. 4.42. The device achieves a low leakage $\sim 10^{10} \text{ A/cm}^2$ and a high current capability over 10^4 A/cm^2 . The differential on resistance without considering current spreading is $\sim 0.1 \text{ m}\Omega/\text{cm}^2$. The turn-on voltage slightly higher than the impurity-doped device since the junction is in the graded AlGaIn layer rather than GaN . A nearly-ideal ideality factor of ~ 1.1 is achieved. The reverse I - V characteristics are shown in Fig. 4.43. With BFP, the device exhibits a $BV \sim 1240 \text{ V}$ and the temperature dependent BV measurement shows that BV increases with the temperature, a signature of avalanche breakdown, whereas this trend was not observed in the first generation of devices.

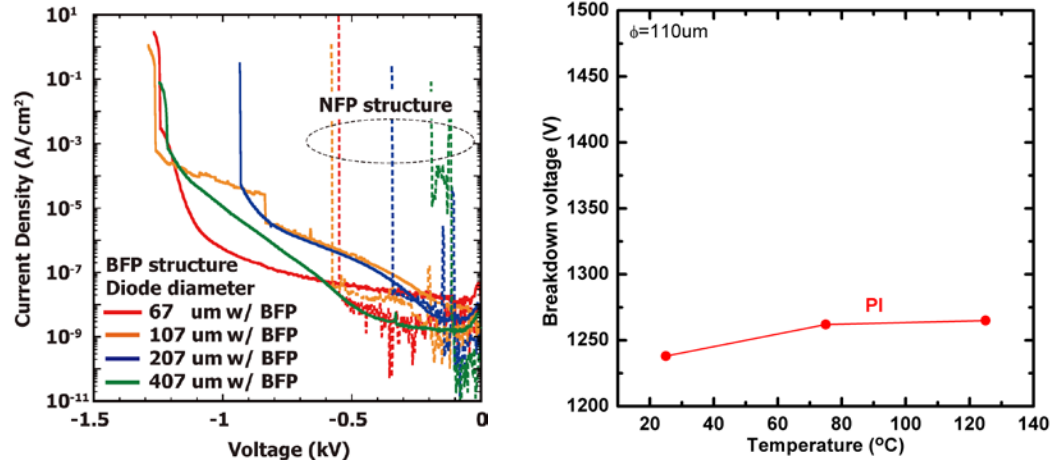


Figure 4.43 (a) Reverse I - V characteristics of *Pi-doped* GaN p-n junction diodes w/o FP and w/ BFP for diodes with different diameters and (b) temperature dependent breakdown voltage characteristics of *Pi-doped* p-n diodes, suggesting an avalanche breakdown. [Courtesy of Dr. Kazuki Nomoto]

CHAPTER 5

POLARIZATION-DOPED SUPER JUNCTION POWER DEVICES

GaN based power devices have attracted great attentions due to its high breakdown field and high electron mobility. Remarkable progresses on GaN based power devices have been achieved recently by several groups on GaN-on-Si or GaN-on-GaN platform [103],[27], [28], [87], [88], [104]–[106],[107], [108], on the way to approach the unipolar tradeoff limit of breakdown-voltage and on-resistance of GaN. The super-junction concept, which is based on charge compensation in the drift region using fully balanced n and p pillar regions, has been widely adopted in Si power device to break such tradeoff between breakdown-voltage and specific on-resistance [109]–[111]. Thus the combination of the material advantage of GaN and the super-junction concept would further improve GaN based device performance. GaN super junction devices using impurity doping [112] or natural super junction [113] based on the polarization sheet charge have been studied to beat the aforementioned limit. However, impurity doping to form p type pillar in GaN still remains a great challenge due to the high activation of Mg in GaN (~170-200 meV); furthermore, practical solutions for device fabrication has also not been proposed yet. The natural super junction has a high electric field crowding problem due to the high sheet charge of the 2 dimension electron gas (2DEG) and 2 dimension hole gas (2DHG) (similar to the field crowding near the gate on the drain side in HEMTs), thus only device performance far less than expected has been reported to date. An innovative technology to realize GaN super junction devices is highly desirable.

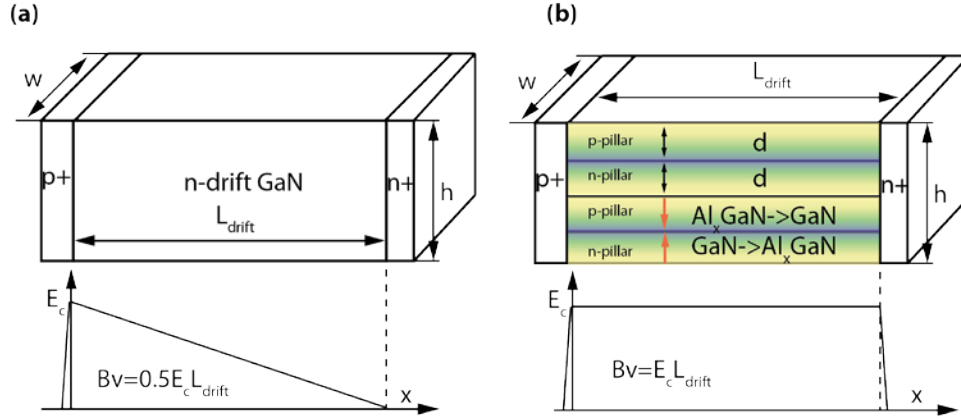


Figure 5.1 Conventional p-n diodes (a) and lateral polarization-doped super-junction (PolarSJ) diodes (b). The top figures show the device structures and dimensions and the bottom figures compare the electric field distribution. The flat electric field profile in LPSJ results from the balanced charge in the drift region thus a higher V_{br} for the same R_{on} [122].

5.1 Lateral Polarization-doped Super Junction

Here we propose a lateral polarization-doped super junction (LPSJ) shown in Fig. 5.1 (b): the n/p pillar regions are realized by compositionally grading AlGaIn, and the n^+ and p^+ cathode/anode regions are formed by regrowth to connect with the n and p pillars, respectively. First, it is important to note that the high spontaneous and piezoelectric polarization charges in the GaN family are absent in Si and SiC. This unique feature is the key enabler for the proposed LPSJ. Second, both n and p type polarization doping as well as n^+ and p^+ regrowth has been demonstrated by our group [12], [13], [114], [115]. More recently, polarization-doped p-n junctions have been also demonstrated by several groups including our own [116],[117]. To realize the super junction, i.e. n/p pillars with balanced charges, one only needs to linearly grade from GaN to $Al_x GaN$ and then grade back to GaN during epitaxial growth, without

any ion implantation process. The doping profile of the pillars can be precisely controlled by MBE/MOCVD growth in terms of Al composition and layer thickness, thus suppressing the charge imbalance problem. Since the charges are spread over the graded layers, the field crowding effect due to the high carrier densities in NSJ can be avoided.

5.2 1D Analytical Modeling of BV and $R_{on,sp}$

For 1D modeling of LPSJ, the specific on resistance R_{on,sp_L} can be expressed as

$$\begin{aligned} R_{on,sp_L} &= \frac{1}{q\mu N_D} \times \frac{L_{drift}}{wh'} \times A = \frac{1}{q\mu N_D} \times \frac{L_{drift}}{wh'} \times wL_{drift} \\ &= \frac{1}{q\mu N_D} \times \frac{L_{drift}^2}{wh'} \end{aligned} \quad (5.1)$$

where h' is the effective electron conducting thickness for each n-pillar considering the depletion at both sides from the nearby p-pillars

$$h' = m(d - d_{dep}) \quad (5.2)$$

and the total thickness

$$h = 2md \quad (5.3)$$

The total depletion width of at the p-n junction is

$$d_{dep} = \sqrt{\frac{2\epsilon_s V_{bi}}{q} \left(\frac{1}{N_A} + \frac{1}{N_D} \right)} \quad (5.4)$$

where the n-pillar/p-pillar doping concentration N_A/N_D are the same since both pillars have the same thickness and grading compositions

$$N_A = N_D = \frac{\sigma_\pi}{d} \quad (5.5)$$

The built-in voltage can be expressed as:

$$V_{bi} = \frac{K_B T}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \quad (5.6)$$

Since for 1D modeling, ideal flat electric field distribution is assumed, then we can get

$$BV = E_c L_{drift} \quad (5.7)$$

With all the information above, we can get the specific on-resistance R_{on,sp_L}

$$R_{on,sp_L} = \frac{BV^2}{q\sigma_\pi \mu E_c^2} \times \frac{2d^2}{h(d-d_{dep})} \quad (5.8)$$

where μ is the average electron mobility for the grading layer. Since the carrier mobility is Al composition dependent as shown in Fig. 4. 3(b), it varies along the vertical direction. An average mobility has been used to calculate $R_{on,sp}$ for the lateral current flow. The average mobility in the graded AlGaN n-pillars can be thus obtained by

$$\frac{1}{\mu} = \frac{\int \frac{n(y)}{\mu(y)} dy}{\int n(y) dy} \quad (5.9).$$

E.g. in a linearly graded Al_xGaN with $x_{Al}=0 \rightarrow 10\%$, an average electron mobility of 1073 cm²/(V·s) is obtained; for a pillar thickness of 560 nm, the polarization doping concentration is $\sim 2 \times 10^{16}$ cm⁻³.

For conventional GaN lateral p-n diodes, $R_{on,sp}$ can be expressed as

$$R_{on,sp_L} = \frac{8}{\epsilon_s \mu h} \times \frac{BV^3}{E_c^4} \quad (5.10)$$

where μ is the electron mobility in the Si-doped GaN drift layer, which has been modeled in the previous section as shown in Fig. 4. 3 (a). The mobility in Si-doped GaN is $\sim 1000-1600$ cm²/ (V·s) for $n \sim 1 \times 10^{16}-1 \times 10^{17}$ cm⁻³.

The ideal specific on-resistance and breakdown voltage between the conventional p-n junction and the LPSJ with linearly graded Al_xGaN pillars ($x_{\text{Al}} = 0 \rightarrow 30\%$) are compared in Fig. 5.2(a), where the total height h of $4\text{ }\mu\text{m}$ and a critical electric field E_C of 3.6 MV/cm are used. It is observed that for $BV > 300\text{ V}$, the LPSJ offers significantly lower $R_{on,sp}$; for instance, a $>10\times$ reduction in $R_{on,sp}$ is predicted around 1200 V and a $>100\times$ reduction in $R_{on,sp}$ for 10 kV . Fig. 5.2 (b) shows the $R_{on,sp}$ as a function of the pillar width d , where in general a smaller pillar width results in a lower $R_{on,sp}$. This is expected since for the same compositional grading range, a small pillar width leads to a high carrier concentration, thus a low $R_{on,sp}$. An optimized pillar width of $\sim 200\text{ nm}$ is found for linearly graded Al_xGaN pillars with $x_{\text{Al}} = 0 \rightarrow 20\%$, which is mainly attributed to the fact that the total depletion width in the n-region becomes comparable with or smaller than the pillar width d when d is $< 200\text{ nm}$. The field crowding in the NSJ and the LPSJ is compared in Fig. 5.3. According to the NSJ theory, there are hole/electron sheet charges of large concentrations at the interface between GaN and AlGaIn, top AlGaIn surface and bottom GaN surface as shown in Figure 5.3(a), which results in severe electric field crowding at the corresponding $p^+/2\text{DEG}$ and $n^+/2\text{DHG}$ junctions shown in Fig. 5.3(c-d) and highlighted by the insets therein. On the other hand, the charges are uniformly distributed in the n and p-pillars of the LPSJ, therefore, the electric field crowding problem was significantly suppressed; e.g. the insets show $>2\times$ reduction in the peak electric field.

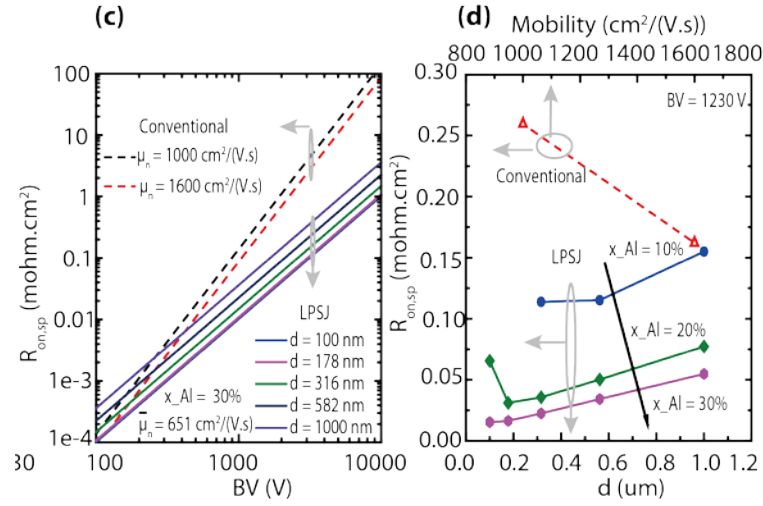


Figure 5.2 (a) Comparison of $R_{on}-BV$ between the impurity-doped conventional junction and the polarization-doped super junction with the pillars linearly graded from GaN to $Al_{0.3}GaN$. For $BV > 300$ V, the LPSJ offers a substantially lower $R_{on,sp}$ than the conventional p-n junctions. (b) Dependence of $R_{on,sp}$ on the pillar width d . Near 1200 V, $\sim 10\times$ lower $R_{on,sp}$ can be achieved in a LPSJ than the conventional junctions (red triangles). An optimal pillar width of ~ 200 nm is predicted for $Al_{x=0\rightarrow 20\%}$ GaN pillars [122].

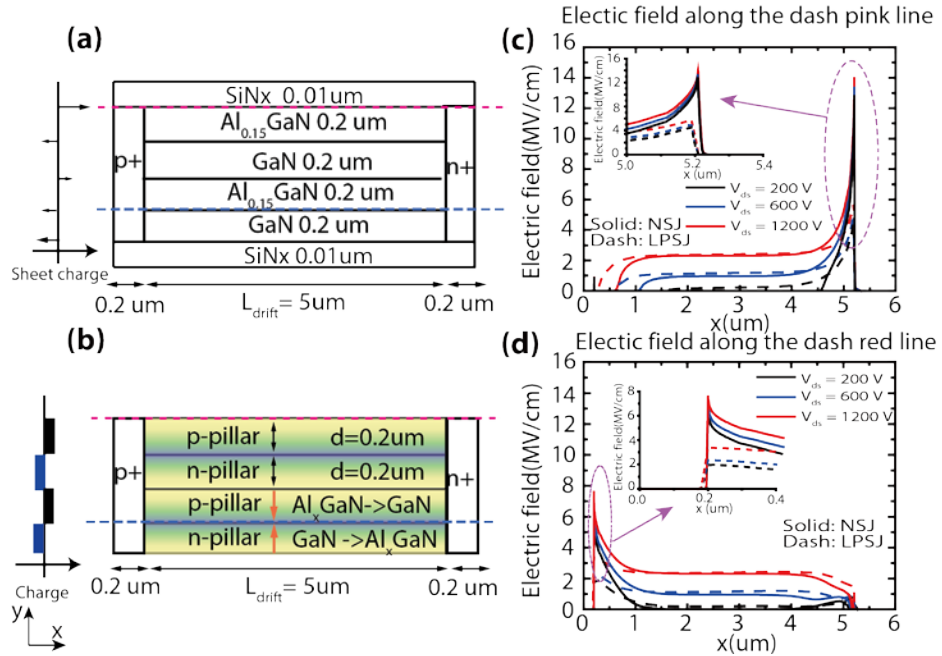


Figure 5.3 The drift region charge distribution along the vertical direction in a NSJ (a) and a LPSJ (b) with the same dimensions, and the simulated electric field distribution along the top surface marked by a pink dash line (c) and along a junction inside the device marked by a blue dash line (d). The insert shown in (c) and (d) indicate severe electric field crowding in NSJ while the peak electric field in LPSJ is at least 2x smaller [122].

5.3 2D Analytical Modeling of BV

The 1D modeling of BV and Ron,sp_L gives us the confidence that the GaN LPSJ has great potential. But the estimation is pretty crude and we may overestimate the advantages, which is mainly due to the approximation of electric field profile. As we can see from Figure 5.3, the electric field is not flat along the entire drift region. There is also peak near the p+/n-pillar region, since there is no charge-balance at this region due to the additional charge at the p+ region. Thus, a more accurate modeling of the electric field profile and BV is needed to better access the performance limits and the design space as well. In this section, a 2D analytical modeling of the electric field and breakdown voltage of GaN LPSJs is presented[118]. Design optimizations in terms of the n/p pillar doping, thickness and x_{Al} composition are discussed.

5.3.1 Case Under Charge Balance

The LPSJ is represented in Fig. 5.4 (a). The unit cell of the LPSJ is shown in Fig. 5.4 (b), where both n and p pillars have a thickness of d , the length of the drift region is L_d , the doping concentrations can be expressed as

$$n=p=N_a=N_d = \sigma_\pi/d \quad (5.11)$$

where σ_π is the net polarization charge in Al_xGaN (cm^{-2}). So the unit cell, consisting of a pair of n/p pillars with balanced charges shown in Fig. 5.4 (b), can be treated in the same fashion as traditional p-n super-junction in terms of electric field profile modeling. When the LPSJ is under reverse bias, there is depletion in the n/p pillars in both lateral and vertical directions, eventually leading to a full depletion in the drift region. Due to the symmetry of LPSJ, the electric field profile is symmetric along the

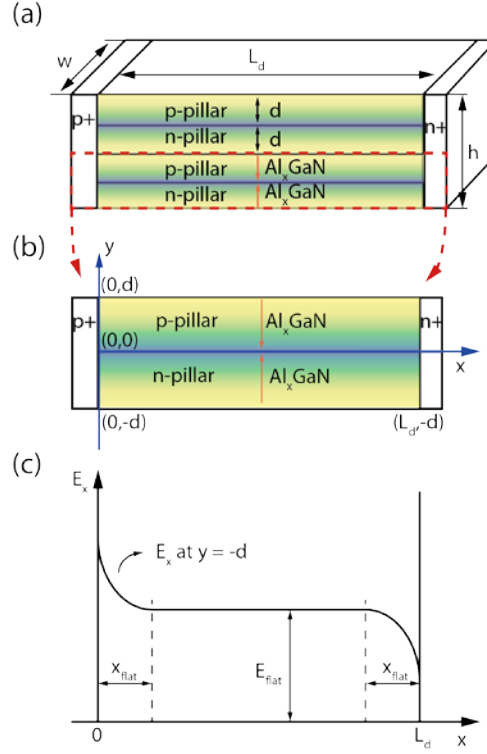


Figure 5.4: (a) Schematic view of the LPSJ structure, (b) the unit cell of LPSJ, (c) the electric field distribution along the x direction at $y = -d$ in a LPSJ showing the peak field E_{max} occurs at $x=0$ [118].

center line of the structure. Strollo et al. established an exact analytical solution for the electric field along $y=-d$ when n/p pillars are fully depleted[119],

$$E(x)|_{y=-d} = -2 \frac{V^* x}{L_d^2} + \frac{V_r + V^*}{L_d} + \sum_{n=1}^{\infty} \frac{K_n \gamma_n}{2} \frac{\cos(K_n x)}{\cosh(K_n(-d))} \quad (5.12)$$

Where $V^* = (qN / 2\epsilon_s) L_d^2$, $K_n = n\pi / L_d$, $\gamma_n = 8V^* / (n\pi)^3 [(-1)^n - 1]$

$\gamma_n = 8V^* / (n\pi)^3 [(-1)^n - 1]$ and V_r is the applied reversed voltage. The schematic electric field profile along the x direction at $y = -d$ is also showing in Fig. 5.4 (c), where the peak maximum electric field E_{max} occurs at $x = 0$ and $y = -d$. When $0 < d/L_d$

<1 , which will be the case in our discussion where the thin n and p pillar can be easily controlled by the MBE/MOCVD epitaxy growth, the maximum electric field at $x = 0$ can be approximated to be [120]

$$E_{\max} = E_{flat} + \frac{qN}{2\epsilon_s} \times 1.66d, \quad (5.13)$$

where $E_{flat} = \frac{V_r}{L_d}$, which is from the flat electric field distribution when n/p are fully depleted (Fig. 5.4(c)), thus it can be treated as the electric field in the i-region of a p-i-n diode.

In order to calculate the breakdown voltage, we need to use the ionization integral along the critical electric field path (i.e. the peak electric field path), where using Eqn. 5.12 can be challenging. On the other hand, this electric field profile can be also modeled using a polynomial approximation [121]

$$E = \left\{ \begin{array}{l} E_{flat} + \frac{qN}{\epsilon_s} \cdot \frac{(x - x_{flat})^m}{mx_{flat}^{m-1}}, x \in [0, x_{flat}] \\ E_{flat}, x \in [x_{flat}, L_d - x_{flat}] \\ E_{flat} - \frac{qN}{\epsilon_s} \cdot \frac{(x - x_{flat})^m}{mx_{flat}^{m-1}}, x \in [L_d - x_{flat}, L_d] \end{array} \right\} \quad (5.14)$$

The maximum electric field along $y = -d$ is at $x = 0$

$$E_{\max} = E_{flat} + \frac{qN}{\epsilon_s} \times \frac{x_{flat}}{m} \quad (5.15)$$

Comparing the E_{\max} expressions in Eq. 5.12 and Eq. 5.15, we can get

$$x_{flat} = 0.83md \quad (5.16)$$

The only fitting parameter m can be obtained by fitting the electric field profile simulated by Sentaurus. For a range of feasible N_d and d values, $m = 3$ resulted in the best fitting (Fig. 5.5). Thus, we can find the electric field along $y = -d$

$$E = \begin{cases} E_{flat} + \frac{qN}{\epsilon_s} \cdot \frac{(x - x_{flat})^3}{3x_{flat}^2}, x \in [0, x_{flat}] \\ E_{flat}, x \in [x_{flat}, L_d - x_{flat}] \\ E_{flat} - \frac{qN}{\epsilon_s} \cdot \frac{(x - x_{flat})^3}{3x_{flat}^2}, x \in [L_d - x_{flat}, L_d] \end{cases} \quad (5.17)$$

The breakdown voltage (BV) can then be found by solving the impact ionization integral

$$\int_0^{L_d} \alpha dx = 1 \quad (5.18)$$

where impact ionization rate $a = 1.5 \times 10^{-42} E^7$ is used[94] .

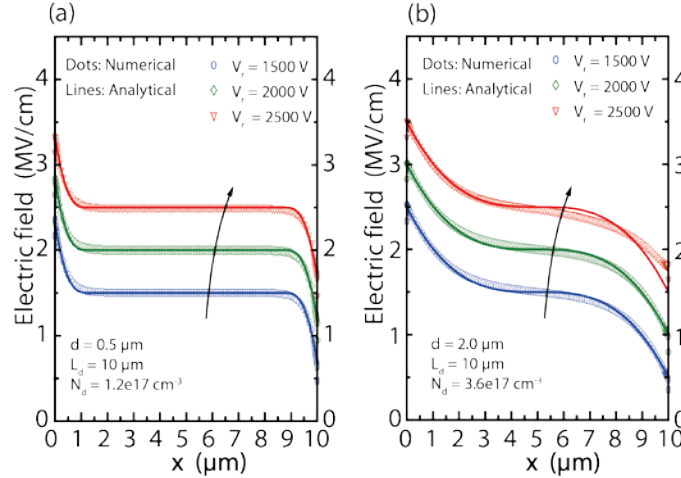


Figure 5.5 Electric field distribution comparison between modeled and numerical simulation along $y=-d$ under different d , N_d values where $L_d=10 \mu\text{m}$: (a) $d = 0.5 \mu\text{m}$, $N_d = 1.2 \times 10^{17} \text{ cm}^{-3}$ and (b) $d = 2.0 \mu\text{m}$, $N_d = 3.6 \times 10^{16} \text{ cm}^{-3}$ [118].

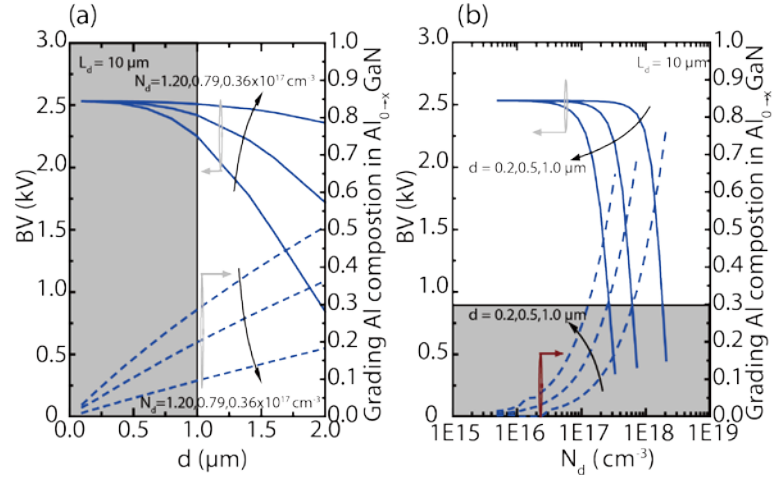


Figure 5.6 Breakdown voltage dependence on (a) pillar width d and (b) doping concentration N_d and its associated x_{Al} at $L_d = 10 \mu\text{m}$. Breakdown voltage reduces with higher doping and larger pillar width. The shaded region ($d \leq 1 \mu\text{m}$, $x_{Al} \leq 0.3$) denotes our feasible growth region at present[118].

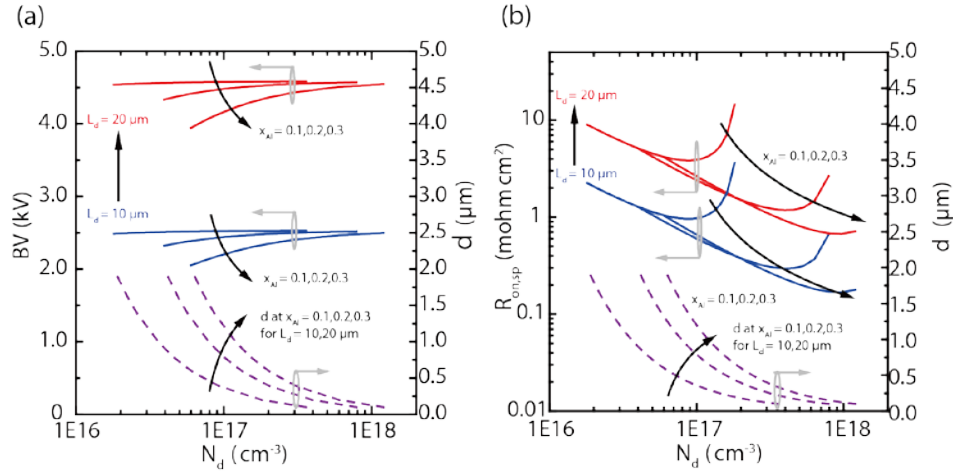


Figure 5.7 (a) Breakdown voltage BV and (b) $R_{on,sp}$ dependence on N_d for various $\text{Al}_x\text{Ga}_{1-x}\text{N}$ ($x_{Al} = 0.1, 0.2, 0.3$) and L_d (10, 20 μm) with the total pillar height $h = 4 \mu\text{m}$. The dashed lines depict the associated pillar thickness d . BV slightly increases with smaller d and higher N_d . $R_{on,sp}$ reduces with increasing x_{Al} . A minimum $R_{on,sp}$ is observed with respect to doping, mobility, and effective conducting area for a given x_{Al} [118].

The $R_{on,sp}$ of the LPSJ considering only unipolar current conducting in the undepleted n pillar region can be expressed as

$$R_{on,sp} = \frac{L_d^2}{q \bar{\mu} N_d} \frac{2d}{h(d - d_{dep})} \quad (5.19)$$

where $\bar{\mu}$ is the average mobility in the graded AlGaIn layer, h is the total height of the LPSJ pillar stacks and d_{dep} is the depletion region in the n pillar region.

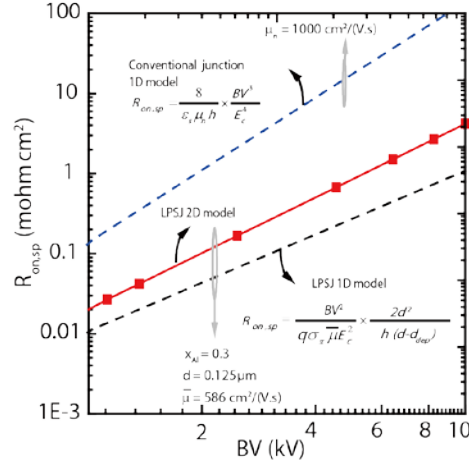


Figure 5.8 Comparison of $R_{on,sp}$ - BV between GaN conventional junction with 1D model and LPSJ with 1D and 2D model. LPSJ 2D model shows >10x reduction in $R_{on,sp}$ over conventional junction for $BV > 2 \text{ kV}$, and a more accurate performance limit over LPSJ 1D model[118].

The BV dependence on the pillar width d , doping concentration N_d and the associated x_{Al} is shown in Fig. 5.6 for a fixed drift region length $L_d = 10 \mu\text{m}$. BV is lower for both larger d and higher N_d , which is expected because the n/p pillars are hard to be fully depleted, thus the super-junction will act more like a traditional abrupt p-n junction with field crowding at the P+/n and N+/p junctions, thus leading to lower BV . Since the doping of the n/p pillar region is controlled by the Al composition in the $\text{Al}_x\text{Ga}_{1-x}\text{N}$, with a higher doping and larger pillar width, a high x_{Al} is needed to get the associated charge. The x_{Al} value at the corresponding doping and pillar width is also shown in Fig. 5.6. For example, with a doping of $1.2 \times 10^{17} \text{ cm}^{-3}$ and a pillar width

of 2 μm , we need to grade from GaN to $\text{Al}_{0.5}\text{GaN}$ over 2 μm . While based on our ongoing experimental development, grading a high Al composition over a thick layer is challenging. The shaded region with $d \leq 1 \mu\text{m}$ and $x_{\text{Al}} \leq 0.3$ in Fig. 5.6 denotes the practical design space based on the known device epitaxial growth conditions today.

Besides dialing the traditional knobs such as the doping and pillar thickness, the Al composition x_{Al} of the Al_xGaN is other unique parameter we can adjust. Fig. 5.7 (a) shows the calculated BV for 3 different x_{Al} values 0.1 to 0.3 while varying d to change N_d . BV is slightly higher with a smaller d and a higher N_d for a lower x_{Al} where the total charge is low and the fully depletion can be easy to meet. While for a higher x_{Al} , the total charge in the n/p pillar is higher, and along with a larger pillar width, full depletion is difficult to reach before the device breaks down. As a result, we see a large change in BV when the pillar width increases from 0.1 to 2 μm . For example, BV is found to be $\sim 2050 \text{ V}$ for $N_d = 6 \times 10^{16} \text{ cm}^{-3}$, $d = 2 \mu\text{m}$ and increases to $\sim 2500 \text{ V}$ for $N_d = 1.2 \times 10^{18} \text{ cm}^{-3}$, $d = 0.1 \mu\text{m}$, while x_{Al} is 0.3 and $L_d = 10 \mu\text{m}$. Since the effective electron mobility in the graded layer depends on the Al composition and the resultant doping concentration, an average mobility considering the alloy scattering and optical phonon scattering is used to model $R_{\text{on},sp}$ as shows in Fig. 5.7(b). The overall trend is that with a higher x_{Al} composition, a lower $R_{\text{on},sp}$ can be obtained since it results in a higher carrier concentration in the conducting pillars though the electron mobility is lower due to the enhanced alloy scattering. Besides, $R_{\text{on},sp}$ shows a minimum for a given x_{Al} due to the tradeoff among doping concentration, carrier mobility and effective conducting area.

The tradeoff relationship between BV and $R_{on,sp}$ for conventional GaN impurity-doped junctions and LPSJ with the 1D (simplified 1D [122]) and 2D (improved, this work) analytical model is compared in Fig. 5.8. For instance, the $R_{on,sp}$ of LPSJ with $x_{Al} = 0.3$ shows $> 10x$ reduction over conventional junctions for $BV > 2$ kV. Since the 2D analytical model represents a more realistic performance limit than the simplified 1D model, which is attributed to a more accurate modeling of the electric field and calculating BV by impact ionization integral, it provides useful guidelines for the development of LPSJ and the design criteria to achieve minimum $R_{on,sp}$.

5.3.2 Case under Charge Imbalance

Since the super junction concept relies on the charge compensation principle, it is crucial to have opposite charges in the n/p pillars perfectly balanced to truly take advantage of the benefits in this structure. However, it is very difficult even in Si SJ process and devices in reality, not to mention the GaN materials. For example, the SIMS results shows a high impurity incorporation such as C in the n-pillar which can be acted as a deep acceptor and H in the p-pillar which can passivate the Mg and prevent Mg to be ionized [123]. All these factors contribute to the charge imbalance. Besides, the fluctuation of Al in the graded layer due to non-idea control would also results in charge profile deviates from the expected profile. Charge imbalance problem would significantly degrade the breakdown voltage of super junction devices as discussed and demonstrated in Si and SiC [121], [124], [125]. In this section, the LPSJ under charge imbalance cases are discussed and modeled.

We use similar method as discussed aforementioned to model the degradation of BV due to charge imbalance. The main change comes from the fact that we need to

remodel the electric field profile along the critical path due to the charge imbalance. As we can see in Fig. 5.10, the electric field profile at the critical path under charge balanced ($p=1.0 \times n$) and imbalanced ($p=0.9 \times n$, $p=0.8 \times n$) case shows a significant difference in the middle of the drift region. For the charge balanced case, the electric field is flat due to the charge balance, where significant sloped electric field profile has been observed in the charge imbalance case. The sloped profile is due to the imbalance charge thus resulting net charge in that region and the slope is given by $((q|p - n|)/(2\epsilon))$. Thus the peak electric field would be enhanced due to this additional sloped profile at the drift region. Similar to the charge balance case, the electric field distribution in a charge imbalanced case can be modeled as

$$E = \left\{ \begin{array}{l} E_{slope} + \frac{q \max(N, P)}{\epsilon_s} \cdot \frac{(x - x_{flat})^3}{3x_{flat}^2}, x \in [0, x_{flat}] \\ E_{slope}, x \in [x_{flat}, L_d - x_{flat}] \\ E_{slope} - \frac{q \max(N, P)}{\epsilon_s} \cdot \frac{(x - x_{flat})^3}{3x_{flat}^2}, x \in [L_d - x_{flat}, L_d] \end{array} \right\} \quad (5.20)$$

where $E_{slope} = \frac{V_r}{L_d} - \frac{q|P - N|}{2\epsilon_s} (x - \frac{L_d}{2})$ [121]. We can find a reasonable good matching

in Fig. 5.10 when we compare the electric field profile between modeled and numerical simulation along $y = -d$ under charge balanced/imbalanced conditions where $L_d = 10 \mu\text{m}$, $d = 0.5 \mu\text{m}$ and $N_d = 1.2 \times 10^{17} \text{ cm}^{-3}$: (a) $p=n$, (b) $p=0.9 \times n$ and (c) $p=0.8 \times n$. A clear trend is that with higher charge imbalance, the peak electric field at $x = 0 \mu\text{m}$ increases dramatically, for example: 3.4 MV/cm @ 2500 V for $p=n$ case compared to 3.85 MV/cm @ 1873 V for $p=0.8 \times n$ case. Moreover, the electric field

profile with high slope and becomes more close to the profile for a traditional junction device. Thus the breakdown voltage decreases dramatically.

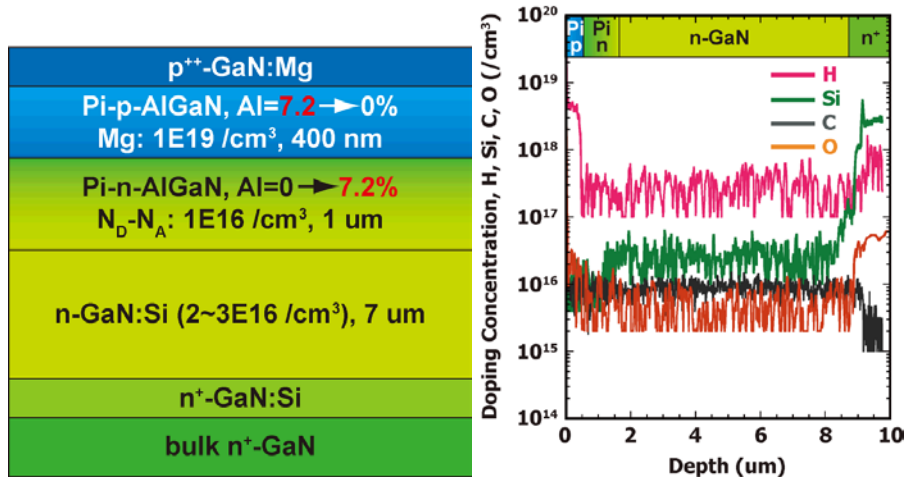
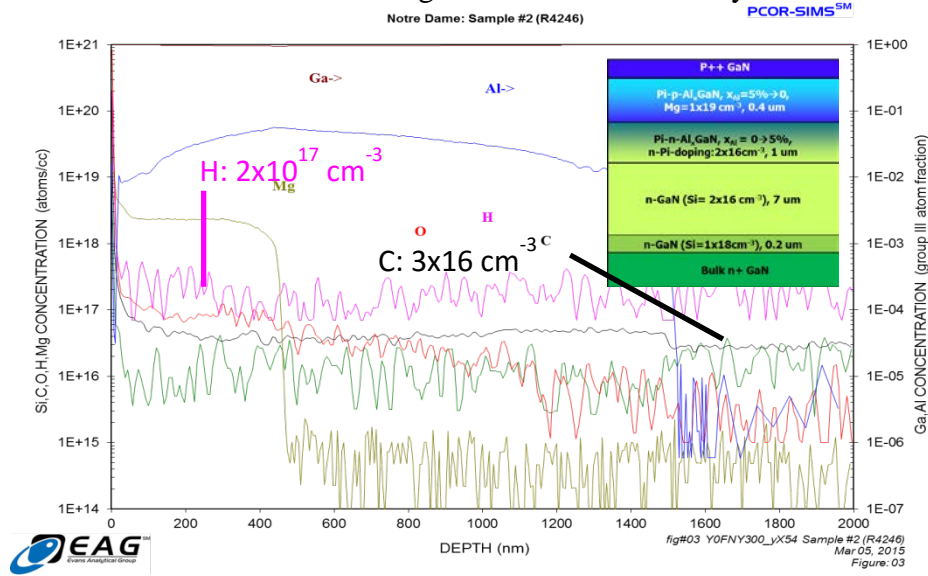


Figure 5.9 H and C, O impurities in GaN p-n diode epitaxial layers, which could contribute to charge imbalance. The upper panel shows hydrogen has a low level of $2 \times 10^{17} \text{ cm}^{-3}$, which may due to the SIMS detection limit. The lower panel shows the SIMS results reproduce from section 4.2.2.3, an apparent hydrogen step in the Mg-doped layer with a high concentration of $> 5 \times 10^{18} \text{ cm}^{-3}$ (SIMS from EAG).

The breakdown voltage can then be found by solving the same impact ionization integral. Fig. 5.11 shows the breakdown voltage at different charge imbalanced case

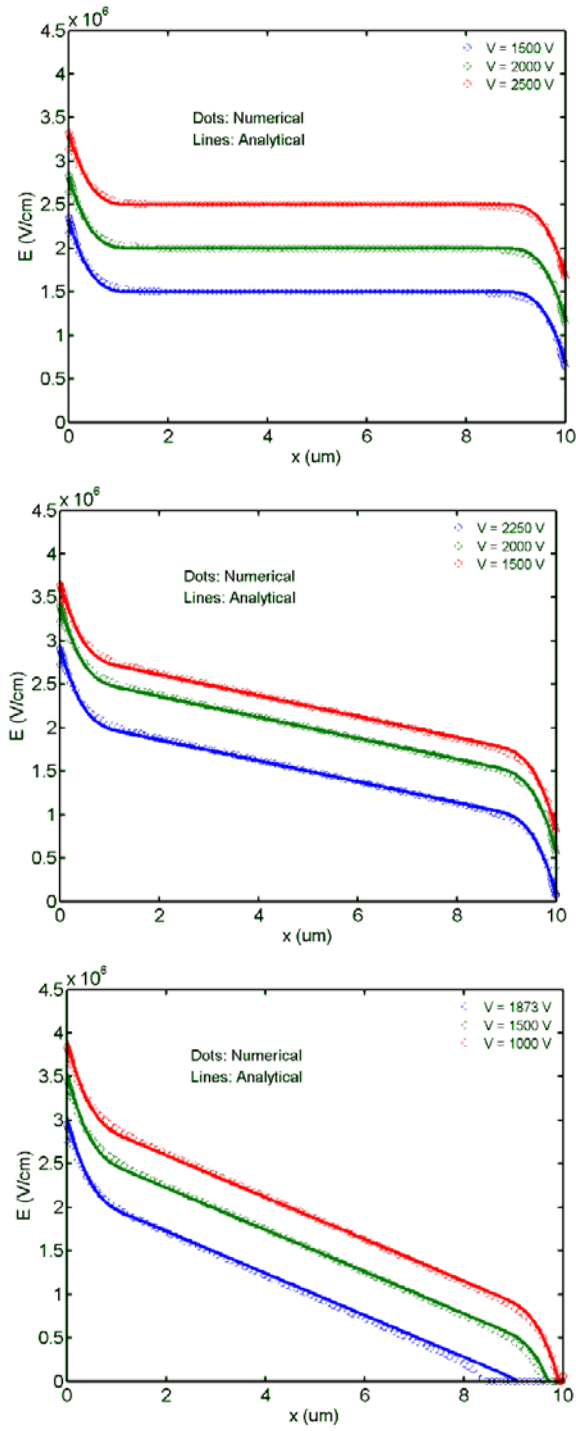


Figure 5.10 Electric field distribution comparison between modeled and numerical simulation along $y = -d$ under charge balanced/imbalanced conditions where $L_d = 10$ μm, $d = 0.5$ μm and $N_d = 1.2 \times 10^{17}$ cm⁻³: (a) $p = n$, and (b) $p = 0.9 \times n$ (c) $p = 0.8 \times n$

for different doping concentrations for $d = 0.5 \mu\text{m}$ and $L_d = 10 \mu\text{m}$ case. Two important features are observed: first, at both doping concentration, when there is charge imbalance, the breakdown voltage would be lower than the charge balanced conditions. Second, when the pillar layer doping concentration is high, the breakdown voltage reduces more significantly by having the charge imbalance percentage ($\sim 5\%$ decrease of BV at $N_d = 3.6 \times 10^{16} \text{cm}^{-3}$ versus $\sim 42\%$ decrease of BV at $N_d = 1.2 \times 10^{17} \text{cm}^{-3}$ for 30% charge imbalance). This is also expected since the net charge at this case is higher, so it results in more sloped electric field profile. While higher doping in the pillar will help to reduce the on-resistance, its breakdown voltage is highly sensitive subject to the charge imbalance. Thus there is another trade-off for the BV design robustness and on-resistance, where the process variation, impurity incorporation etc. need to be fully taken into account.

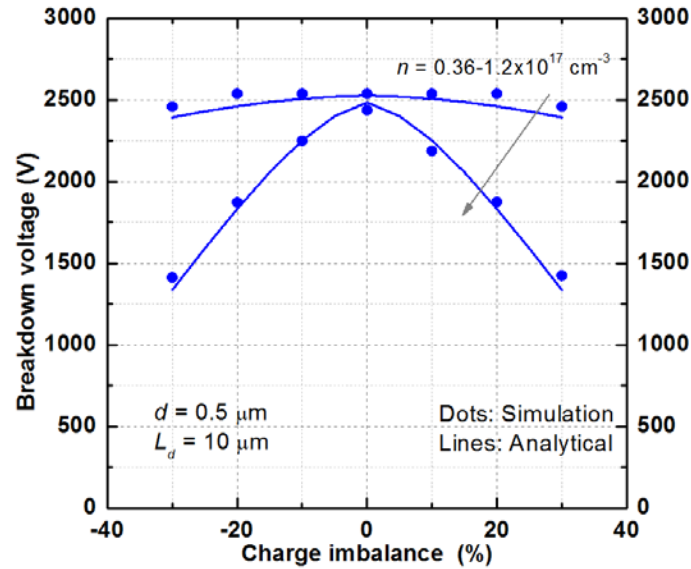


Figure 5.11 BV under charge balanced/imbalanced conditions where $L_d = 10 \mu\text{m}$, $d = 0.5 \mu\text{m}$ for different target pillar doping $N_d = 3.6 \times 10^{16}$ and $1.2 \times 10^{17} \text{cm}^{-3}$.

5.4 Summary

LPSJ featuring charge-balanced n/p-pillars by epitaxially grown graded AlGaIn layers has been proposed. 1D analytical model shows it has great potential to outperform traditional GaN unipolar junction devices. A more detailed 2D analytical modeling of breakdown voltage and on-resistance of GaN lateral LPSJ under charge-balanced conditions has been presented. The breakdown voltage of GaN LPSJ is obtained by solving impact ionization integral along the critical electric field path with the modeling of the electric field. Design examples with BV and minimum $R_{on,sp}$ at different x_{Al} composition have been discussed, providing valuable guidelines for the development of LPSJ. Moreover, the effects of charge imbalance on reducing the breakdown voltage of the devices are also modeled. It shows with a high pillar doping concentration, the charge imbalance will dramatically reduce the breakdown voltage up to 42% for a charge imbalance of 30% when $L_d=10\text{ }\mu\text{m}$, $d=0.5\text{ }\mu\text{m}$ with a target pillar doping is $N_d=1.2\times10^{17}\text{ cm}^{-3}$.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

In this work, the development and optimization of GaN based devices for high speed RF application as well as high power switching applications are discussed, which are mainly focused on best utilizing polarization induced charges at the GaN heterojunction (2DEG at interfaces) and graded AlGaIn layers (*Pi-doping* in bulk layers).

For high speed RF applications, the ultimate limitations on the speed of GaN HEMTs with T-gates have been investigated. The aggressive gate length scaling and optimization of GaN HEMTs with regrown contacts and high gate stem T-gates have led to boost the device speed >300 GHz, on its way to approach THz electron devices. Besides, special attention should be paid to T-gate HEMTs with an ultra-scaled source drain distance. The additional fringing capacitance due to coupling from the source/drain to the T-gate cap would increase the total capacitance, though the source drain distance scaling does reduce the parasitic resistance. The extrinsic delay is found to be a significant (and ultimate) factor in limiting the speed in ultra-scaled GaN HEMTs, and is fundamentally determined by the device intrinsic g_m and the fringing capacitance between the gate stem and the access regions. Thus improving g_m by enhancing the channel injection velocity with further device scaling is key in realizing THz GaN devices.

AlGaIn/GaN HEMTs on Si with non-alloyed regrown ohmic contacts show a

record-low leakage current, about six orders of magnitude smaller than that of the conventional devices with alloyed ohmics. Meanwhile it also processes minimum current dispersion compared to the devices with alloyed contacts. The breakdown voltage also boosts more than 50%. This provides new thoughts in the GaN HEMT development to preserve the high quality GaN pristine surface by avoiding the surface directly exposed to high temperature processes.

For power switching applications, polarization-induced doping by linearly grading Al composition in AlGa_N to form n and p type doping layer have been integrated into the design of GaN power devices. Analytical study suggests that by linearly grading GaN to Al_x0Ga_N with Al_x0Ga_N situated at the highest field region of the device, the ideal $R_{on,sp}$ of the *Pi-doped* device can be $1/3 - 2/3$ of that of the *Imp-doped* device. Experimental data shows with high-quality GaN substrates and epitaxial layers, a vertical impurity-doped GaN p-n diode can achieve a breakdown voltage of 1.7 kV with avalanche breakdown capability and $R_{on,sp}$ of $0.55 \text{ m}\Omega\cdot\text{cm}^2$ with considering the current spreading of $10 \text{ }\mu\text{m}$ for a $10 \text{ }\mu\text{m}$ drift layer. The on-wafer measurement of reverse recovery time of the GaN p-n diode shows an ultrafast time $\sim 2 \text{ ns}$, which indicates it is much suitable for high-speed power switching applications. The extracted minority hole lifetime in the n-drift region is $\sim 2.3 \text{ ns}$. Thus the conduction modulation in the drift layer is expected to be low and make it challenging for realizing extremely high-voltage high-current GaN devices, i.e. unipolar and bipolar devices have similar differential R_{on} . With a proper impurity control, *Pi-doped* GaN p-n diodes shows a breakdown voltage of $\sim 1.25 \text{ kV}$ and $R_{on,sp}$ of $0.1 \text{ m}\Omega\cdot\text{cm}^2$ with a $1 \text{ }\mu\text{m}$ *Pi-doped* layer by grading GaN to Al_{0.07}GaN at the junction on top of a $7 \text{ }\mu\text{m}$ drift

impurity-doped layer. This translates to a higher “apparent” critical breakdown field of 2.43 MV/cm compared to 1.91 MV/cm to that of the control *Imp-doped* GaN p-n diode.

To further improve the performance of GaN based power devices, LPSJ featuring charge-balanced n/p-pillars by epitaxially grown graded AlGaIn layers has been proposed. A 2D analytical modeling of breakdown voltage and on-resistance of GaN LPSJ under charge-balanced conditions has been presented. The breakdown voltage of GaN LPSJ is obtained by solving the impact ionization integral along the critical electric field path with the modeling of the electric field. Design examples with BV and minimum $R_{on,sp}$ at different Al compositions x_{Al} have been discussed, providing valuable guidelines for the development of LPSJ. Moreover, the effects of charge imbalance on reducing the breakdown voltage of the devices are also modeled. The charge imbalance will dramatically reduce the breakdown voltage up to 42% for a charge imbalance of 30% when $L_d = 10 \mu\text{m}$, $d = 0.5 \mu\text{m}$ with a target pillar doping of $N_d = 1.2 \times 10^{17} \text{ cm}^{-3}$.

6.2 Future Work

6.2.1 Large Signal Performance of GaN HEMTs

GaN transistors are on the way to replace GaAs transistors and Si LDMOS for RF power amplifications ranging from mm-wave satellite/radar communication to advanced LTE base station wireless infrastructures due to the high efficiency, wide bandwidth and high power gain. The large-signal high-RF-power performance is crucial for these applications. Thus a careful characterization and optimization of the power performance are needed. For such applications, typically the device will

require a breakdown voltage > 40 V for a > 20 V operation voltage, thus optimization of the breakdown voltage by employing filed plate at source and/or gate drain side are important without significantly degradation the RF performance. Besides, the effects of the non-alloyed regrown contacts on current dispersion and long term stability need to be accessed under high RF power conditions.

6.2.2 PolarMOS

Vertical GaN power transistors enabled by polarization doping are the ultimate high-speed power devices, e.g. PolarMOS as shown in Figure 6.1. The device epitaxial layer structure consists of a drift region (lightly doped n-GaN (green) either by impurity or polarization-induced n-type ($n \sim 1 \times 10^{16} \text{ cm}^{-3}$), the top layer polarization-induced p-type Al_xGaN , a thin AlGaIn layer grown on top of a thin unintentionally doped GaN channel and the polarization-doped p-AlGaIn underneath. It features a high threshold $V_{th} > 2\text{V}$ by employing a gate dielectric layer, ~ 10 nm $\text{Al}_{x<0.2}\text{GaIn}$ top barrier, ~ 10 nm UID GaN channel, a polarization doped p-layer bottom barrier. Since the channel is situated in as-grown epitaxial layers, a high mobility, thus a high current capability is expected. Besides, it is easier to convert a polarization-doped p-layer to n-type by ion implantation. Further, an added benefit of a $\text{p-Al}_{0->x}\text{GaIn}/\text{n-Al}_{x->0}\text{GaIn}$ junction is that the p-n junction depletion falls in the AlGaIn layer, since AlGaIn has a higher bandgap than GaN, its critical electrical field is expected to be higher than that of GaN. The simulation results suggest the

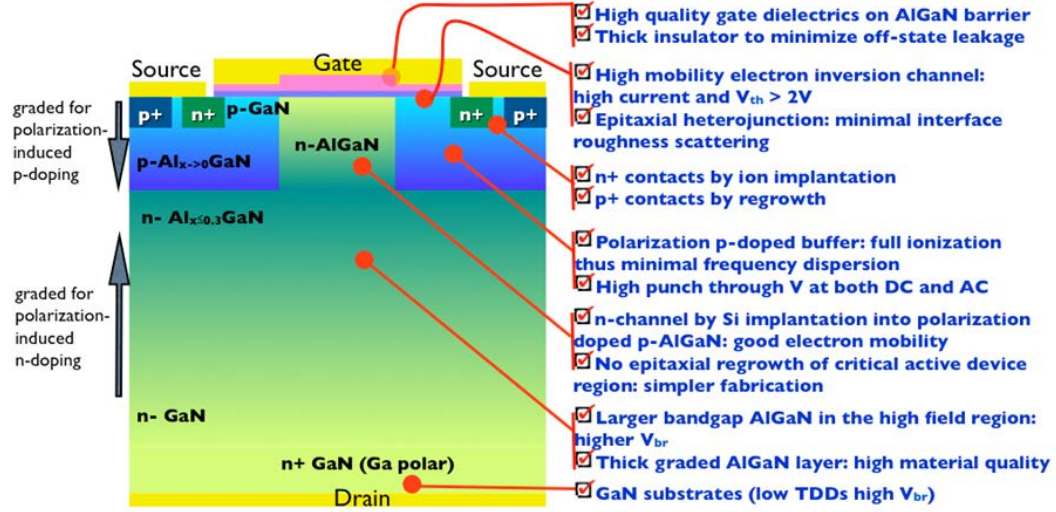


Figure 6.1 The ultimate GaN power device-PolarMOS featuring: a larger bandgap AlGa_N in the high field region to achieve higher breakdown voltages, a polarization p-doped buffer to achieve fully ionization, thus minimizing frequency dispersion and achieving high punch-through voltages at both DC and AC, a high mobility electron inversion channel for high current and an adjustable threshold voltage $> 2V$ [36].

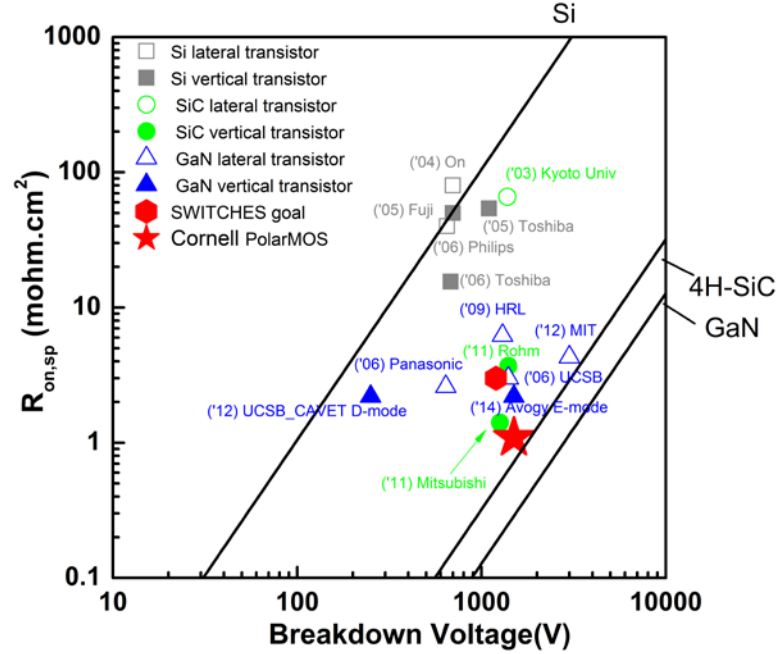


Figure 6.2 Comparison of power transistors near V_{br} of 1000 V. With advanced device architecture such as IGBT and super junction MOS, Si devices surpasses the theoretical limit of unipolar devices. Both SiC and GaN power transistors exhibit room for improvement. PolarMOS stands out compared to other solutions, promising a better $V_{br}^2/R_{on,sp}$ metric close to the theoretical limit of unipolar SiC power devices[36].

PolarMOS stands out compared to other solutions in the same neighborhood of the voltage and current of the state-of-the-art power devices, promising a better $V_{br}^2/R_{on,sp}$ metric close to the theoretical limit of simple unipolar SiC power devices.

6.2.3 Beyond GaN: Ga₂O₃ Power Devices

Owing to the large bandgap, breakdown electric field (E_b) and high carrier mobility, wide-bandgap semiconductor (e.g. SiC and GaN) based power devices have been extensively studied for next-generation power-switching applications. Recently, a new wide-bandgap oxide semiconductor, gallium oxide (β -Ga₂O₃), has attracted attention for power-switching applications because it has an extremely large bandgap of 4.5~4.9 eV enabling a high breakdown voltage (V_{br}) and a high Baliga's figure of merit [126]. Furthermore, large-area and high-quality bulk substrates of Ga₂O₃ can be grown by low-cost methods, which remain a significant challenge for both SiC and GaN. Schottky barrier diodes (SBDs), with a low turn-on voltage and a fast switching speed due to majority carrier conduction, are ideal candidates for high-power and high-speed rectifiers. Recently, Higashiwaki et al. have demonstrated excellent device results, which includes SBDs with $V_{br} \sim 115$ V on (010) Ga₂O₃ substrates (with a net doping concentration $N_D-N_A \sim 5 \times 10^{16} \text{ cm}^{-3}$) [127] and SBDs with epitaxial Si-doped n-Ga₂O₃ drift layers ($N_D-N_A \sim 1.4 \times 10^{16} \text{ cm}^{-3}$) grown by HVPE on (001) Ga₂O₃ substrates with $V_{br} \sim 500$ V [128]. Oishi et al reported Ni-based SBDs on (-201) Ga₂O₃ with a $N_D-N_A \sim 1 \times 10^{17} \text{ cm}^{-3}$ and $V_{br} \sim 40$ V [129]. However, no high voltage ($V_{br} > 100$ V) devices have been reported yet on (-201) Ga₂O₃, the crystal orientation readily available in up to 4 inch diameter wafer. As an initial exploration step, we fabricated

Pt-based SBDs on unintentionally-doped (UID) (-201) n-type Ga₂O₃ substrates with $V_{br} > 100$ V[130].

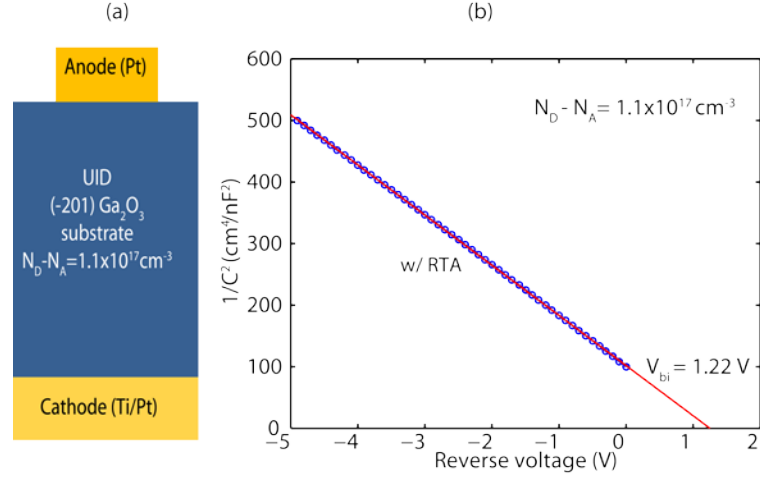


Figure 6.3 (a) Schematic cross section of SBDs on (-201) Ga₂O₃ substrate and (b) $1/C^2$ - V characteristics of Ga₂O₃ SBDs w/ RTA showing net doping concentration $\sim 1.1 \times 10^{17} \text{ cm}^{-3}$ built-in voltage ~ 1.22 V[130].

Figure 6.3 shows the schematic cross section and the $1/C^2$ - V plot of the fabricated Ga₂O₃ SBDs. The net doping concentration ($N_D - N_A$) in the (-201) Ga₂O₃ substrates extracted by the $d(1/C^2)/dV$ method is $\sim 1.1 \times 10^{17} \text{ cm}^{-3}$. The built-in potential extracted from the $1/C^2$ -vs- V plot is $V_{bi} \sim 1.22$ V as shown in Figure 6.3 (b). The substrate thickness is $\sim 680 \text{ }\mu\text{m}$ and the resistivity is $\sim 6.3 \text{ }\Omega/\text{sq}$. The top circular Schottky anode electrodes with diameters of $50 \text{ }\mu\text{m}$ and $390 \text{ }\mu\text{m}$ were fabricated on Ga₂O₃ substrates by photolithographic patterning, followed by evaporation of Pt (80 nm) as anode metal, and liftoff. The back cathode is formed by evaporation of a Ti (50 nm)/Pt (100 nm) metal stack. A rapid thermal annealing (RTA) process at $470 \text{ }^\circ\text{C}$ in N₂ ambient for 60 s is applied to devices labeled as w/ RTA. No additional surface passivation or field plate is employed for the devices studied in this work. The $50 \text{ }\mu\text{m}$ and $390 \text{ }\mu\text{m}$ diameter diodes were used for current density-voltage (I - V) and capacitance-voltage

(C-V) measurements, respectively. All measurements were performed at room temperature.

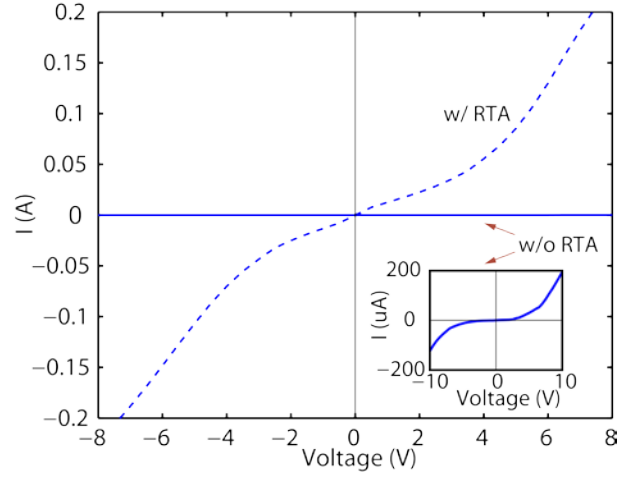


Figure 6.4 I - V curves measured between two contacts at the backside of on (-201) Ga_2O_3 substrate with Ti/Pt and the metal stacks at w/o and w/ RTA process conditions[130].

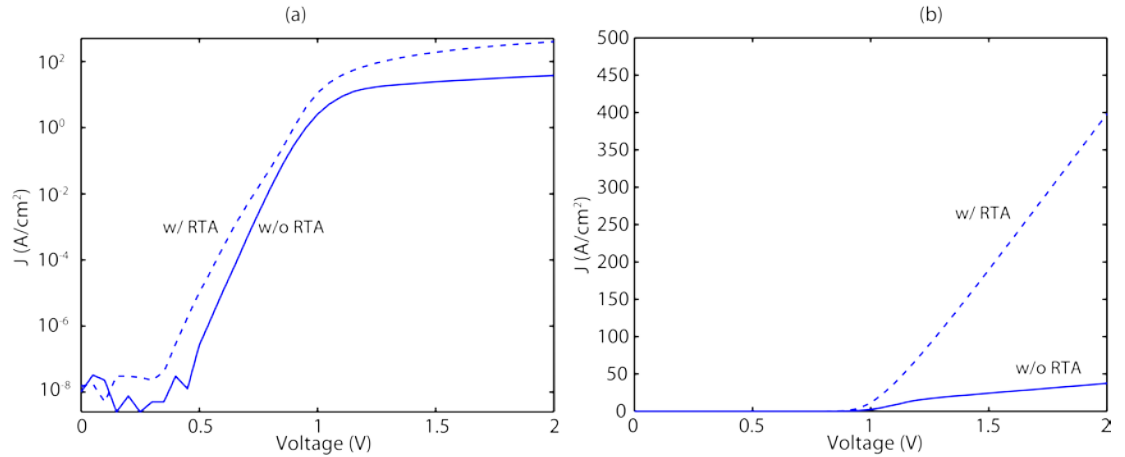


Figure 6.5 Forward J - V characteristics of Ga_2O_3 SBD w/o and w/ RTA process plotted in (a) logarithmic and (b) linear scales. With the RTA process, the back contact dramatically improves, which helps to improve the current density from ~ 34 to 400 A/cm^2 . Near unit ideality factors of 1.02 were obtained for the both SBDs and extracted barrier for SBDs w/o and w/ RTA process is 1.53 and 1.35 eV, respectively[130].

Figure 6.4 shows the I - V curves measured between two back-contacts separated by $\sim 160\ \mu\text{m}$ on a test sample using the same substrate and metal stack w/ and w/o RTA. The contacts fabricated with the RTA process showed a reasonable ohmic behavior with high current capability. On the other hand, the as-deposited metal stack contacts show a Schottky behavior thus allowing only very low currents. The detailed mechanism for this improvement is not yet clear and warrants further investigation.

Figures 6.5 (a) and (b) show the forward J - V characteristics of the SBDs in logarithmic and linear scales, respectively. The turn-on voltage is about 1 V for both cases. Near unity ideality factors of 1.02 are obtained for both SBDs with and without RTA. The extracted Pt/Ga₂O₃ barrier height $q\phi_B$ is 1.53 eV and 1.35 eV for w/o and w/ RTA process, respectively. The Pt/(-201) Ga₂O₃ barrier height extracted here is close to the reported values in the range of 1.3-1.5 eV for Pt/(010) Ga₂O₃ [4]. In Fig.3 (b), the SBD w/ RTA process shows a dramatic improvement in the forward current-carrying capability: from 34 to 400 A/cm² @ 2V. This is most likely a result of the improved back-contact and a reduction of $q\phi_B$. The differential on-resistance R_{on} as determined from the slope of the linear regions in Fig. 3(b) for SBD w/o RTA and w/ RTA is about 29.4 and 2.5 m Ω -cm², respectively. Since the substrate specific resistivity along the current flowing direction is 26.5 m Ω -cm², a R_{on} of 2.5 m Ω -cm² is attributed to current lateral spreading from the top anode to the bottom contact. The reverse J - V characteristics are shown in Figure 6.6 and V_{br} for both SBDs is about 120 V. The hard breakdown observed in both devices at the edge of the anode electrodes is due to electric field crowding. This observation indicates that using edge terminations such as a field plate and/or a guard ring will improve V_{br} . Nonetheless,

the critical surface breakdown field pointing along the $[-201]$ direction can be estimated to be > 2.1 MV/cm.

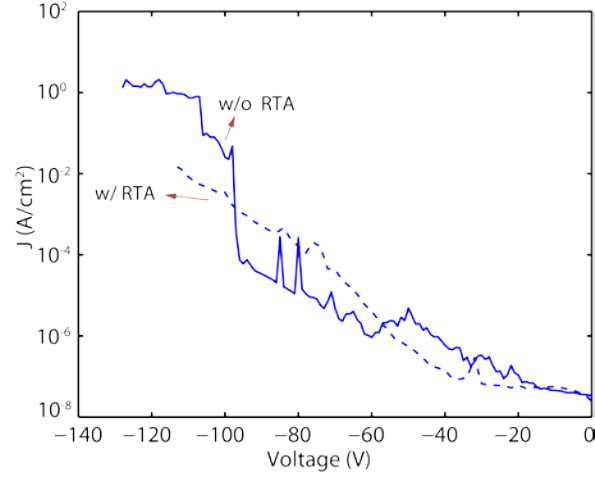


Figure 6.6 Reverse J - V characteristics of Ga_2O_3 SBDs w/o and w/ RTA[130].

In summary, we fabricated $\text{Pt}/\text{Ga}_2\text{O}_3$ SBDs on single-crystal $\beta\text{-Ga}_2\text{O}_3$ (-201) substrates for the first time. Ohmic contacts were obtained on the backside with a RTA process. The $\text{Pt}/\text{Ga}_2\text{O}_3$ SBDs on (-201) substrates show similar behavior with the devices fabricated on (010) Ga_2O_3 substrates.

This work paves way for developing other Ga_2O_3 vertical power devices such as high voltage Ga_2O_3 SBD with UID doped drift layer or hybrid Ga_2O_3 p-i-n diode with Mg-doped GaN as the p region and UID Ga_2O_3 as the drift region.

APPENDIX A

A. DEVICE CHARACTERIZATIONS

A.1 Small Signal RF Measurement and Analysis

For a transistor operating at radio frequency (RF) and microwave frequencies, a two-port network and the associated *S-parameters* are used to characterize the device performance. For a two-port network shown in Fig. A.1, the *S-parameters* between two ports are expressed as

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (\text{A.1})$$

where $b_1 = s_{11}a_1 + s_{12}a_2$ and $b_2 = s_{21}a_1 + s_{22}a_2$

They also satisfy the following relationships

$$\begin{aligned} s_{11} &= \frac{b_1}{a_1} = \frac{V_1^-}{V_1^+} \Big|_{Z_L=Z_0}, \quad s_{12} = \frac{b_1}{a_2} = \frac{V_1^-}{V_2^+} \Big|_{Z_S=Z_0}, \\ s_{21} &= \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+} \Big|_{Z_L=Z_0}, \quad s_{22} = \frac{b_2}{a_2} = \frac{V_2^-}{V_2^+} \Big|_{Z_S=Z_0} \end{aligned} \quad (\text{A.2})$$

where Z_0 , Z_S , Z_L are the characteristic impedance, input and output impedance. s_{11} and s_{22} are the input and output port voltage reflection coefficients, s_{21} is the forward voltage gain and s_{12} is the reverse voltage gain. The *S-parameters* are very powerful tools for design of RF devices and power amplifiers. For RF device characterization, the *s-parameters* can be converted into *H-parameters* to calculate the current gain h_{21} and the maximum unilateral power gain U , thus f_t/f_{\max} where the h_{21}/U reach unity or 0 dB.

$$h_{21} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}s_{21}} \quad (\text{A.3})$$

$$U = \frac{|s_{21}|^2}{(1-|s_{11}|)^2(1-|s_{22}|)^2} \quad (\text{A.4})$$

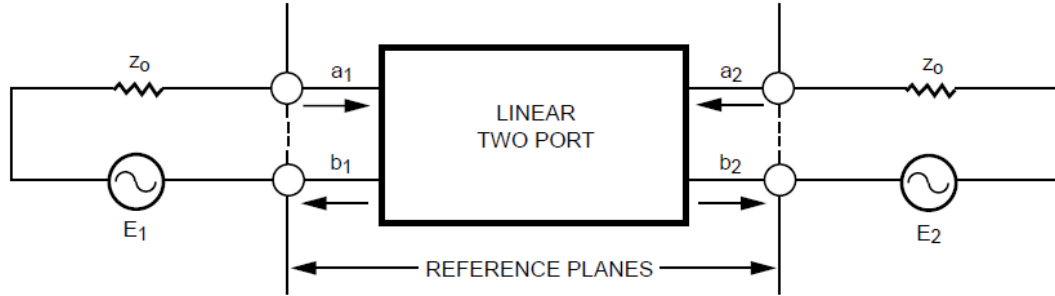


Figure A.1 Two-port network showing incident waves of a_1/a_2 , reflection waves of b_1/b_2 to measure S-parameters [131]

In our lab, the small signal measurement for the two-port *S-parameters* is carried out using an Agilent 8510(Agilent N5250C) vector network analyzer (VNA). The VNA is calibrated using LRM or LRRM off-wafer impedance standards, within the typical frequency range of 0.25-30 GHz (0.1-110 GHz). During the measurement, the transistor is biased at a DC voltage level near its peak g_m , a small ac signal is applied on top of the DC bias in port 1 (gate) at varying frequencies, an associated output ac signal can be detected in port 2 (drain).

The as-measured two-port *s-parameters* of the device under test (DUT) need to be de-embedded to exclude the pads parasitics. This can be realized using the de-embedding process by subtracting the on-wafer OPEN pad parasitic capacitance (converted into admittance Y_1 , Y_2 and Y_3) and SHORT pad inductance (converted into impedance Z_1 ,

Z_2 and Z_3) as shown in Fig. A.2. Then the active device extrinsic impedance after de-embedding is given by

$$Z_A = Z[Y_{DUT} - Y_{open}] - Z[Y_{short} - Y_{open}] \quad (\text{A.5})$$

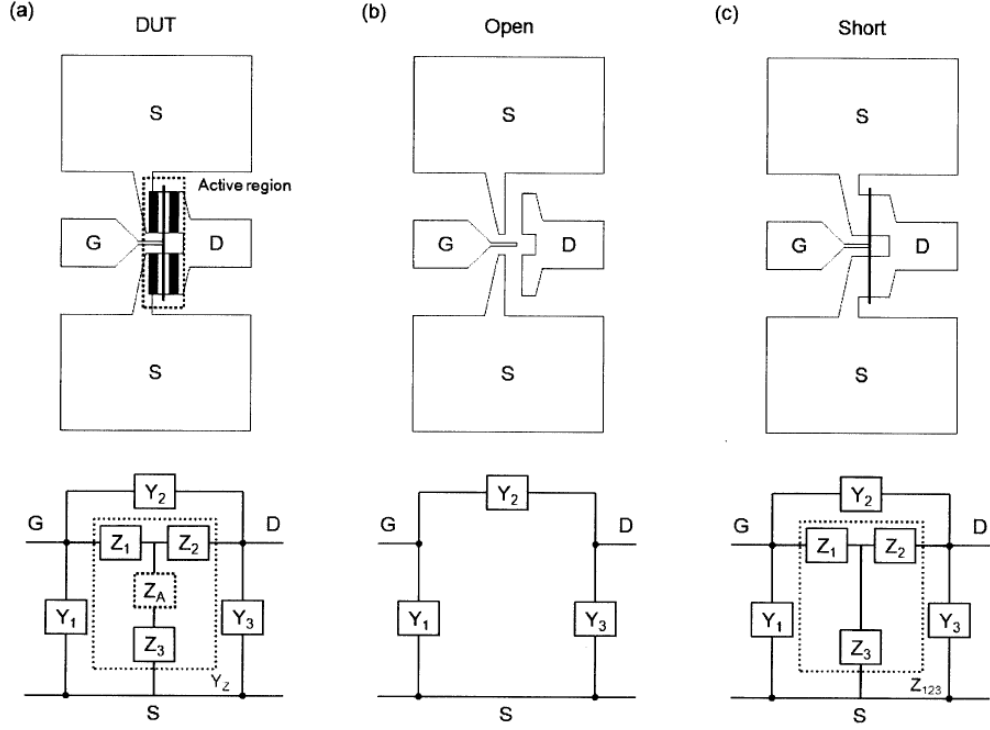


Figure A.2 Two-port S -parameter de-embedding method to obtain the active-device impedance parameters by subtracting the on-wafer OPEN and SHORT, which can then convert to S -parameters [132].

With the measured s -parameters, we can extract f_t/f_{max} of our devices. To gain more detailed understanding, a small signal equivalent circuit is usually used to model the devices as illustrated in Fig. A.3. The intrinsic circuit includes the gate-source capacitance C_{gs} , gate-drain capacitance C_{gd} , drain-source capacitance C_{ds} , input resistance R_i , intrinsic transconductance g_m and output resistance R_{ds} . The intrinsic parameters should be bias dependent. Besides the intrinsic elements, the extrinsic elements include the gate resistances R_g , drain resistance R_d and source resistance R_s .

In addition, each terminal has a pad inductance (L_g , L_d and L_s) and pad capacitance between each two terminals (C_{pgd} , C_{pgs} and C_{pds}). Ideally, the extrinsic parameters should be bias independent.

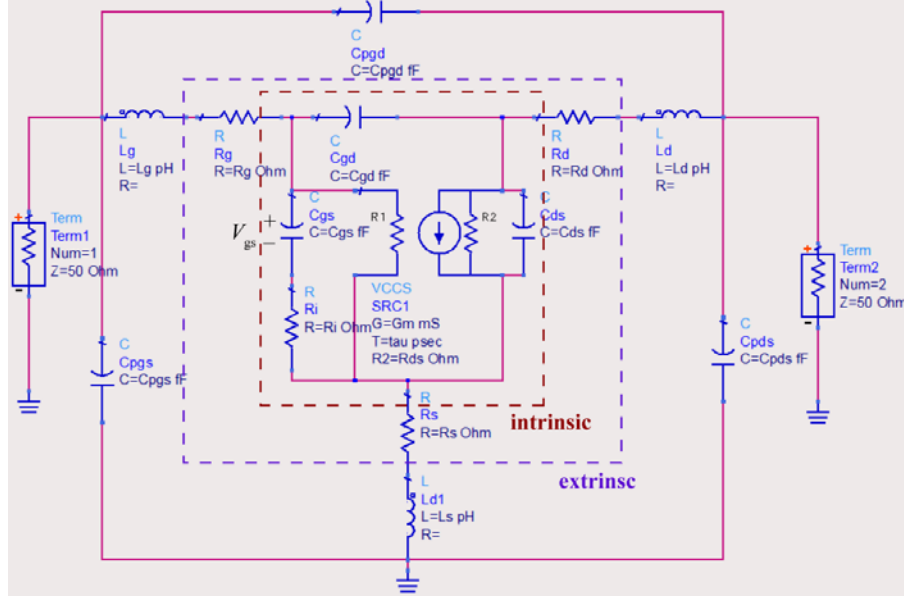


Figure A.3 A representative HEMT small signal equivalent circuit[53].

From the equivalent intrinsic circuit, the current gain can be expressed as

$$|h_{21}| = \left| \frac{i_2}{i_1} \right| \cong \frac{g_m}{\omega(C_{gs} + C_{gd})}, \quad (\text{A.6})$$

then

$$f_T \cong \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (\text{A.7})$$

A more complicate expression of f_T is shown below

$$f_T = \frac{g_m / 2\pi}{(C_{gs} + C_{gd})[1 + (R_s + R_d) / R_{ds}] + g_m C_{gd} (R_s + R_d)} \quad (\text{A.8})$$

where $C_{gs} = C_{gs,int} + C_{gs,ext}$, $C_{gd} = C_{gd,int} + C_{gd,ext}$

f_{max} can be express as

$$f_{\max} \cong \frac{f_T}{2\sqrt{(R_s + R_g + R_i)/R_{ds} + 2\pi f_T R_g C_{gd}}} \quad (\text{A.9})$$

A.2 Pulsed I - V Measurements

The comparison of pulsed and DC I - V measurement setups for a three terminal transistor using Keithley 4200 SCS and 4225 PMU is shown in Fig. A.4. The waveform shown in the DC I - V setup has a 100% duty cycle in static DC I - V measurements, while the duty cycle is typical lower than 5% in pulsed I - V measurements. So self-heating due to the device turn on can be significantly suppressed depends on the pulse width of the applied signals. Besides, we can also use the pulsed I - V to characterize traps in a wide range of devices. When the pulse width is shorter than the trap response time, traps cannot respond to the applied signal and thus we can see differences in I - V curves by applying different pulse width signals to evaluate the effect of traps on device I - V s. In our Keithley system, a minimum pulse width of 300 ns can be reliably applied to the gate and drain terminal separately. Three quiescent bias conditions are routinely used in our pulsed I - V measurements: first, $(V_{dsq}, V_{gsq}) = (0, 0)$ for the cold pulse measurement to eliminate the self-heating effect compared to the DC I - V s; second, $(V_{dsq}, V_{gsq}) = (0, V_{gsq} < V_{th})$ for gate-lag measurement; and third $(V_{dsq}, V_{gsq}) = (\text{high saturation drain bias } V_{ds}, V_{gsq} < V_{th})$ for drain-lag measurement. Fig. A.5 shows a representative plot of a pulsed I - V measurement on a AlGaIn/GaN HEMT with regrown contacts without any passivation measured with a 300 ns pulse width and a 0.5 ms period. We can observe clear

differences under the DC and cold pulse conditions, which may be attributed to self-heating. Besides, we also observe a gate-lag $\sim 19\%$ and a drain-lag of 4% .

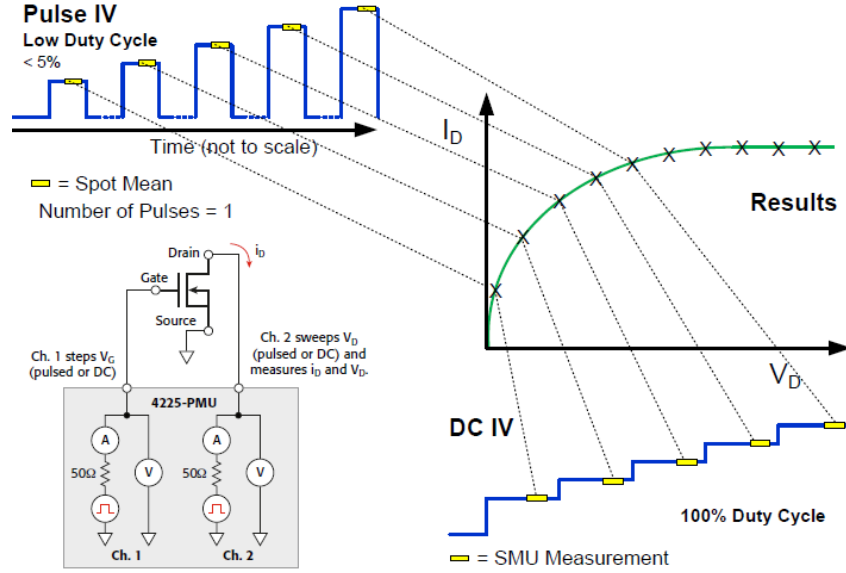


Figure A.4 The pulsed I - V measurement setup using Keithley 4200 SCS and 4225 PMU[53].

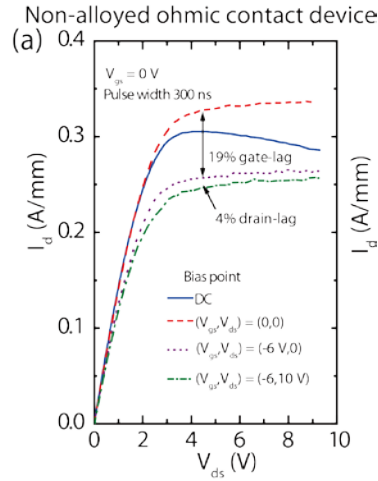


Figure A.5 A representative plot of pulsed I - V measurements on an AlGaN/GaN HEMT with a 300 ns pulse width and a 0.5 ms period.

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